

# WV-4 SIT LOGIC SCHEMATICS

WV-4  
6/27/2016

- 001.TITLE PAGE

002.POWER SEQUENCE

003.CPU(1/16) : DDI/EDP

004.CPU(2/16) : DDR4

005.CPU(3/16) : DDR4

006.CPU(4/16) : MISC/JTAG

007.CPU(5/16) : LPC/SPI/SMBUS/C-LINK

008.CPU(6/16) : LPSS/ISH

009.CPU(7/16) : AUDIO/SDXC

010.CPU(8/16) : PCIE/USB/SATA

011.CPU(9/16) : CSI-2/EMMC

012.CPU(10/16) : CLOCK SIGNALS

013.CPU(11/16) : SYSTEM PM

014.CPU(12/16) : CPU POWER

015.CPU(13/16) : CPU POWER

016.CPU(14/16) : PCH POWER

017.CPU(15/16) : GND

018.CPU(16/16) : CFG/RESERVED

019.XDP CONNECTOR

020.RTC BATTERY

021.SPI FLASH

022.DDR4 SO DIMM

023.TYPE\_C\_CONTROLLER

024.TYPE-C\_MUX

025.BLANK

026.BLANK

027.BLANK

028.DP SWITCH

029.DP DEMUX

030.BLANK

031.BLANK

032.BLANK

033.BLANK

034.BLANK

035.BLANK
- 036.BLANK

037.RF COMPONENT

038.LCD/LID/MIC/CAMERA/PWR SW

039.BLANK

040.HDMI CONNECTOR

041.DISPLAY PORT CONNECTOR

042.BLANK

043.SATA HDD CONN

044.USB POWER/CONN

045.USB POWER/CONN

046.GBE CLARKVILLE

047.GBE LAN SWITCH

048.GBE MAGNETICS

049.RJ45 CONNECTOR

050.PCIE MINI CARD SLOT

051.MEDIA CARD CONTROLLER

052.MEDIA CARD INTERFACE

053.SMART CARD I/F

054.AUDIO ALC3245-GRT

055.AUDIO CONNECTOR

056.AUDIO JACK SENSE

057.AUDIO EXT MIC I/F

058.AUDIO SPEAKER

059.AUDIO BEEP

060.DOCKING CONNECTOR

061.MEC1653(1/3)

062.MEC1653(2/3)

063.MEC1653(3/3)

064.KEYBOARD/TRACK POINT

065.TOUCH PAD/NFC/FPR

066.BLANK

067.FAN CONNECTOR

068.G-SENSOR

069.TPM

070.SMBUS SW/LPC DEBUG PORT
- 071.THINK ENGINE(1/2)

072.THINK ENGINE(2/2)

073.DC-IN

074.BATTERY INPUT

075.BATTERY CHARGER(BQ25700)

076.BLANK

077.BLANK

078.DC/DC VCC5M/VCC3M(TPS51285B)

079.DC/DC IMVP8(NCP81208)

080.DC/DC CPUCORE(NCP81382)

081.DC/DC VCCGFXCORE\_I(NCP81381)

082.DC/DC VCCSA(NCP81380)

083.DC/DC VCC1R0\_SUS(TPS51367R)

084.BLANK

085.DC/DC VCC1R2A(TPS51716)

086.DC/DC VCC1R8\_SUS(RT8068A)

087.BLANK

088.DC/DC VCC2R5A(RT8068A)

089.BLOCK DIAGRAM

090.BLANK

091.BLANK

092.LOAD SW PCH SUS/TRACK POINT

093.LOAD SW LAN

094.LOAD SW CPU

095.LOAD SW B

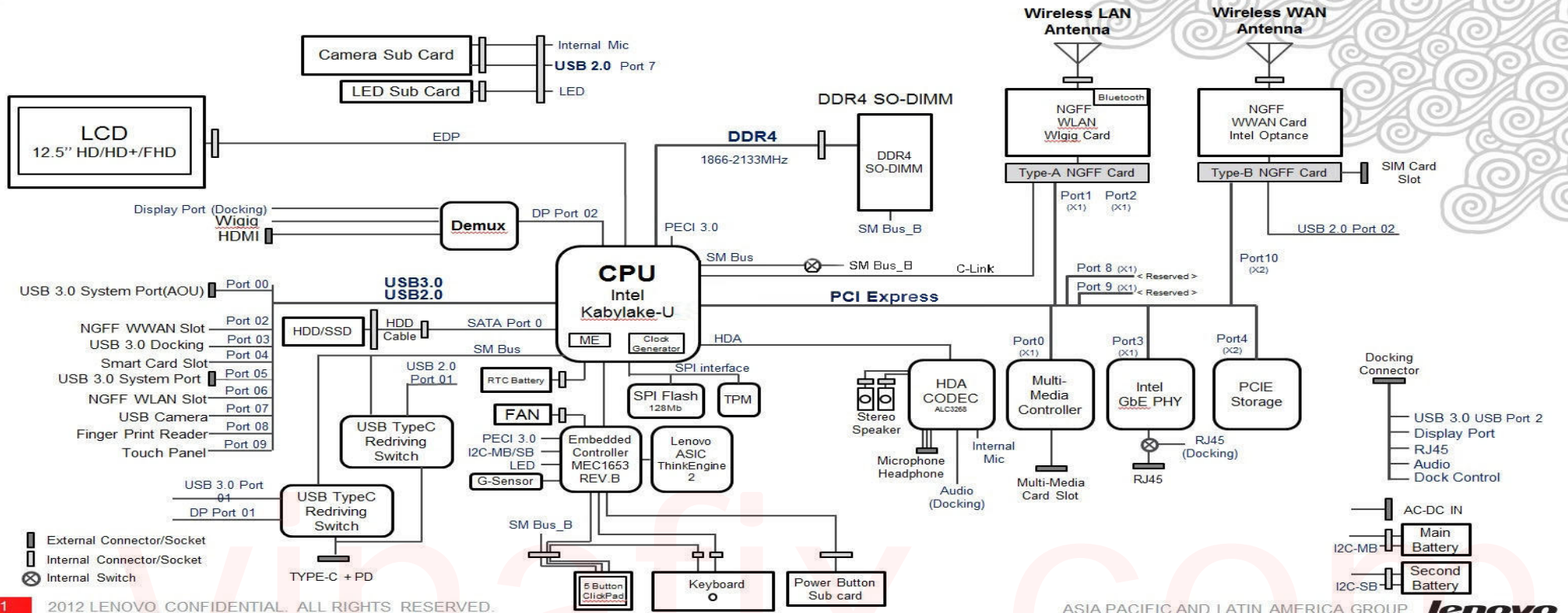
096.LOAD SW WWAN & WLAN

097.BLANK

098.PTH FOR SCREW HOLES

099.BLOCK DIAGRAM

100.NEC LED BOARD



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**Voltage Rails** ( O --> Means ON , X --> Means OFF )

Power Plane	VSYS	VCC3M	VCC1R2A	State
	VCC3SW	VCC5M		
			VCC1R0_SUS (Deep Sleep) VCC3B VCCST_CPU (Deep Sleep) VCCSTG_CPU +VCCSA VCCCFUIO VCCCFUCORE VCC1R8_SUS (Deep Sleep) VCC3_SUS (Deep Sleep) VCCMPHY_GATE VCCGFXCORE_I VCCSTG	
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

**EC SMBus1 address EC SMBus2 address**

Device	Address	Device	Address
G-Sensor (KX023)	0011 110Xb	BATTERY Charger PU101	0x12H (0001001bX)

**PCH SM Bus address PCH SM Bus0 address**

Device	Address	Device	Address
CH-A DDR DIMM0 (J21)	1001 0000b	Intel Lan J219	0XC8
Touch Pad	\$2C	NFC	?????

**EC SMBus0 address EC SMBus7 address**

Device	Address	Device	Address
Main Battery	0x16	Second Battery	0 X16

**EC SMBus5 address**

Device	Address
Type C controller	000B

**BOM Structure Table**

BOM Structure	BTO Item
@	Not stuff
I3@	CPU I3 KABylake U
I5@	CPU I5 KABylake U
I7@	CPU I7 KABylake U
VPRO@	For VPRO part
NVPRO@	For NVPRO part
TI@	For TI TUSB546 Type C Switch
PA@	For Parade 8743 Type C Switch
ME@	ME part(connector, hole)
CONN@	ME part(connector, hole)
RF@	RF component
RF_NS@	RF reserved components
EMC_NS@	EMC reserved components
EMC@	EMC components
KABYU@	For Kabylake use
SKYU@	For skylake U use
SKYI3@	CPU I3 SKYlake U
SKYI5@	CPU I5 SKYlake U
SKYI7@	CPU I7 SKYlake U
SKYI5 VPRO@	For I5 VPRO SKYLAKE CPU
SKYI7 VPRO@	For I7 VPRO SKYLAKE CPU
i5 VPRO@	For I5 VPRO KABYLAKE CPU
i7 VPRO@	For I7 VPRO KABYLAKE CPU

CPU

PCB

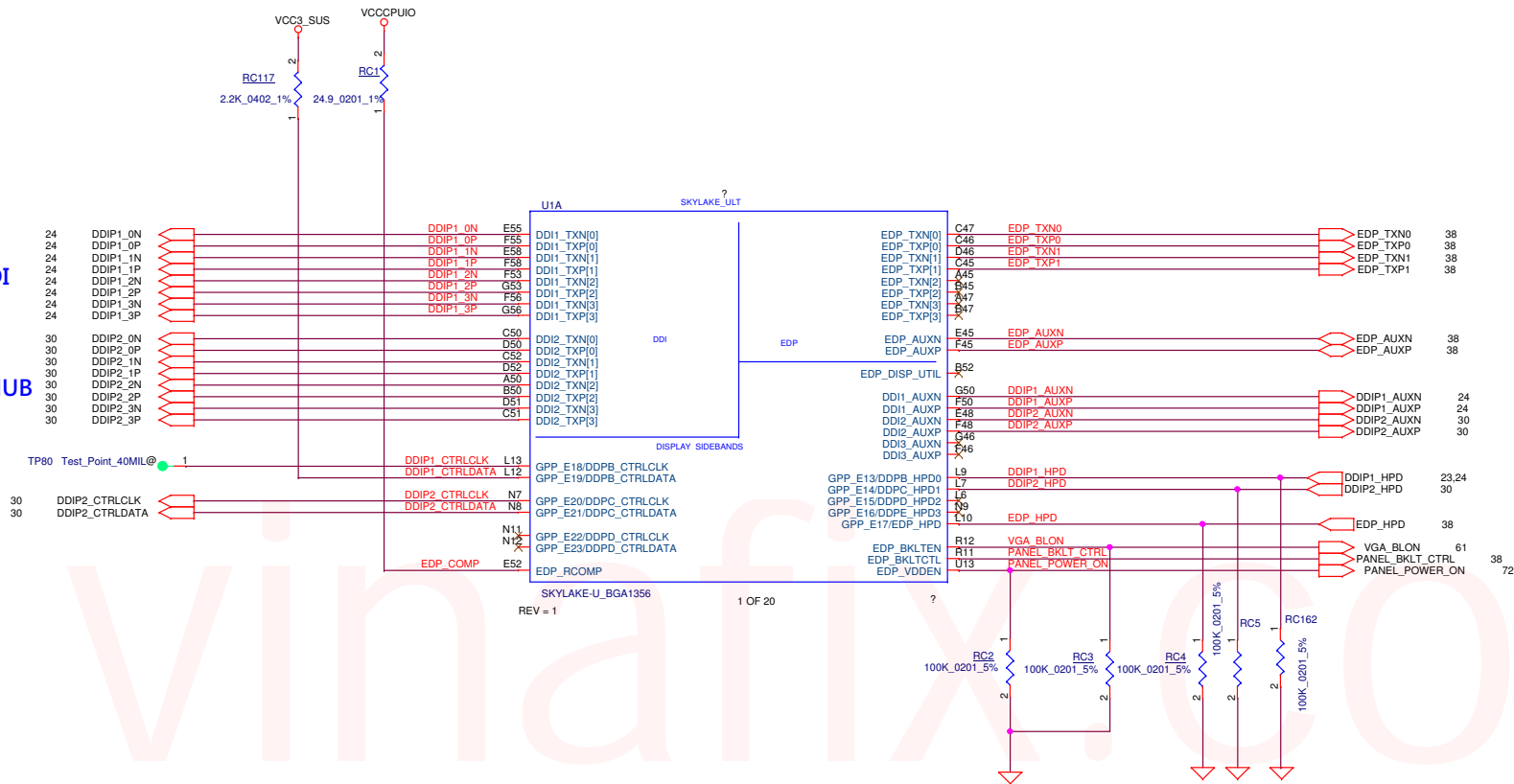
ZZZ

NM-B061

DAZ12F00100

Type C DDI

1 to 3 DP HUB



S IC FJ8067702739738 SR2ZW H0 2.4G 01 I, A.5  
SA000080720  
I3@



S IC FJ8067702739739 SR2ZU H0 2.5G 01 I, A.4  
SA000080320  
I5@



S IC FJ8067702739740 SR2ZV H0 2.7G 01 I, A.4  
SA000080420  
I7@



S IC FJ8067702739633 SR340 H0 2.6G 01 I, A.3  
SA000086M10  
I5 VPRO@



S IC FJ8067702739628 SR33Z H0 2.8G 01 I, A.3  
SA000086N10  
I7 VPRO@



S IC FJ8066201931106 QLB3 D1 2G BGA 1356, A.3  
SA000082E20  
SKYI3@



S IC FJ8066201930409 SR2EY D1 2.3G 01 I, A.3  
SA00007GP30  
SKYI5@



S IC FJ8066201930408 SR2EZ D1 2.5G 01 I, A.3  
SA00007GM30  
SKYI7@



S IC FJ8066201924931 SR2F0 D1 2.4G BGA 1356 01 I, A.3  
SA00007GN20  
SKYI5 VPRO@



S IC FJ8066201924950 SR2F1 D1 2.6G 01 I, A.5  
SA00007GL30  
SKYI7 VPRO@

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Issued Date	2016/2/3	Deciphered Date	2015/08/10
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Title		LCFC	
CPU(1/16) : DDI/EDP			
Size	Document Number	Rev	0.3
Customer	VOLVERINE4 UMA		
Date:	Tuesday, December 20, 2016	Sheet	3 of 100



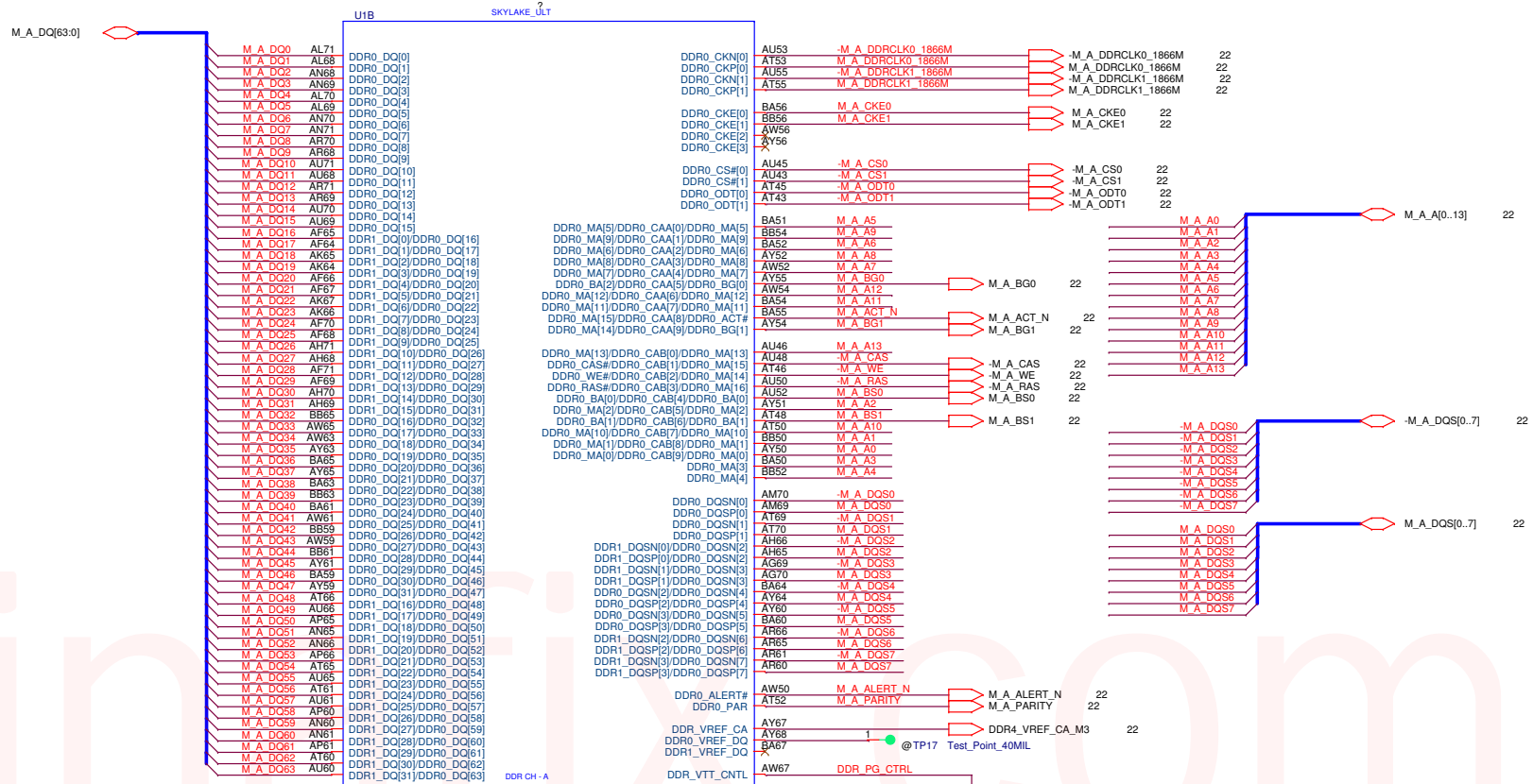
TABLE	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL88	DDR0_DQ[1]	DDR0_DQ[1]
	AN88	DDR0_DQ[2]	DDR0_DQ[2]
	AN89	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL89	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR88	DDR0_DQ[9]	DDR0_DQ[9]
Block 2	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU88	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR89	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU89	DDR0_DQ[15]	DDR0_DQ[15]
	BB86	DDR0_DQ[16]	DDR0_DQ[16]
	AW86	DDR0_DQ[17]	DDR0_DQ[17]
	AY83	DDR0_DQ[18]	DDR0_DQ[18]
	BA86	DDR0_DQ[19]	DDR0_DQ[19]
Block 4	AY85	DDR0_DQ[20]	DDR0_DQ[20]
	BA83	DDR0_DQ[21]	DDR0_DQ[21]
	BB83	DDR0_DQ[22]	DDR0_DQ[22]
	BA81	DDR0_DQ[23]	DDR0_DQ[23]
	AW81	DDR0_DQ[24]	DDR0_DQ[24]
	BB88	DDR0_DQ[25]	DDR0_DQ[25]
	AW88	DDR0_DQ[26]	DDR0_DQ[26]
	BB81	DDR0_DQ[27]	DDR0_DQ[27]
	AY81	DDR0_DQ[28]	DDR0_DQ[28]
	BA88	DDR0_DQ[29]	DDR0_DQ[29]
Block 6	AY89	DDR0_DQ[30]	DDR0_DQ[30]
	AY38	DDR0_DQ[31]	DDR0_DQ[31]
	AW38	DDR0_DQ[32]	DDR0_DQ[32]
	AY37	DDR0_DQ[33]	DDR0_DQ[33]
	BB38	DDR0_DQ[34]	DDR0_DQ[34]
	BA37	DDR0_DQ[35]	DDR0_DQ[35]
	BB37	DDR0_DQ[36]	DDR0_DQ[36]
	AY36	DDR0_DQ[37]	DDR0_DQ[37]
	AW36	DDR0_DQ[38]	DDR0_DQ[38]
	AY33	DDR0_DQ[39]	DDR0_DQ[39]
Block 8	AW33	DDR0_DQ[40]	DDR0_DQ[40]
	BB36	DDR0_DQ[41]	DDR0_DQ[41]
	BA36	DDR0_DQ[42]	DDR0_DQ[42]
	BB33	DDR0_DQ[43]	DDR0_DQ[43]
	AY31	DDR0_DQ[44]	DDR0_DQ[44]
	AW31	DDR0_DQ[45]	DDR0_DQ[45]
	AY29	DDR0_DQ[46]	DDR0_DQ[46]
	AW29	DDR0_DQ[47]	DDR0_DQ[47]
	BB29	DDR0_DQ[48]	DDR0_DQ[48]
	BA27	DDR0_DQ[49]	DDR0_DQ[49]

LOGIC

TABLE

TABLE	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

LOGIC

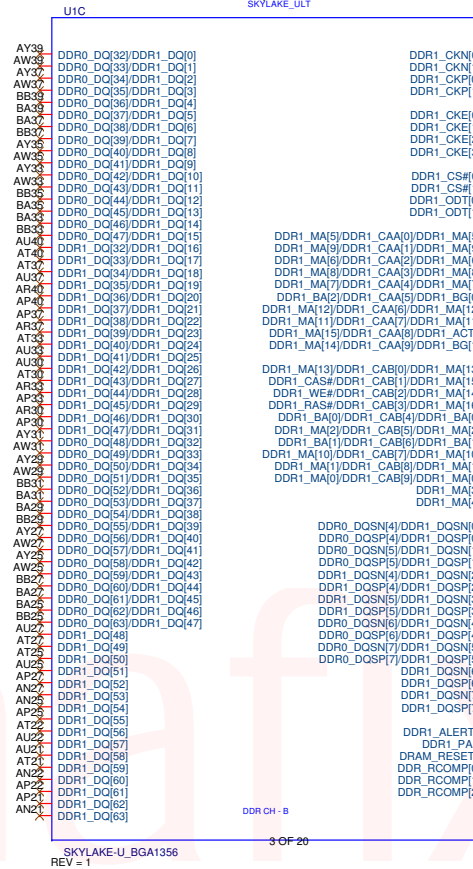


TABLE

TABLE	Pin	DDR3L	LPDDR3	DDR4
Block 0	BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
	BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
	BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
	AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
	AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
	AY55	DDR0_MA[2]	DDR0_CAA[5]	DDR0_BG[0]
Block 2	AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
	BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
	BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
	AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
Block 4	AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
	AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
	AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
	AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
	AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
	AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
Block 6	AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
	AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
	BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
	AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
	BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
	BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

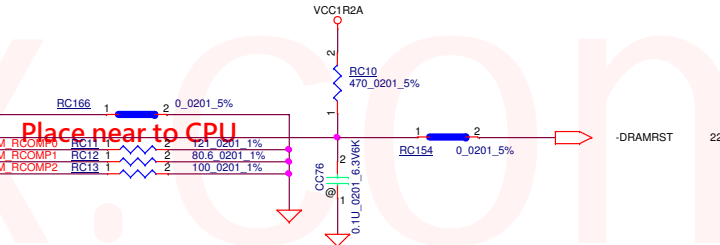
LOGIC

TABLE			
	Pin	Interleave	Non-Interleave
Block 1	AF66	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK66	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF68	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF69	DDR1_DQ[9]	DDR0_DQ[25]
	AK71	DDR1_DQ[10]	DDR0_DQ[26]
	AK68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AK70	DDR1_DQ[14]	DDR0_DQ[30]
	AK69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[32]
	AU66	DDR1_DQ[17]	DDR0_DQ[33]
	AP66	DDR1_DQ[18]	DDR0_DQ[34]
	AN66	DDR1_DQ[19]	DDR0_DQ[35]
	AN68	DDR1_DQ[20]	DDR0_DQ[36]
	AP68	DDR1_DQ[21]	DDR0_DQ[37]
	AT66	DDR1_DQ[22]	DDR0_DQ[38]
	AU66	DDR1_DQ[23]	DDR0_DQ[39]
	AT66	DDR1_DQ[24]	DDR0_DQ[40]
	AU61	DDR1_DQ[25]	DDR0_DQ[41]
	AP60	DDR1_DQ[26]	DDR0_DQ[42]
	AN60	DDR1_DQ[27]	DDR0_DQ[43]
	AN61	DDR1_DQ[28]	DDR0_DQ[44]
	AP61	DDR1_DQ[29]	DDR0_DQ[45]
	AT60	DDR1_DQ[30]	DDR0_DQ[46]
	AU60	DDR1_DQ[31]	DDR0_DQ[47]
Block 5	AU46	DDR1_DQ[32]	DDR1_DQ[48]
	AT46	DDR1_DQ[33]	DDR1_DQ[49]
	AT37	DDR1_DQ[34]	DDR1_DQ[50]
	AU37	DDR1_DQ[35]	DDR1_DQ[51]
	AR46	DDR1_DQ[36]	DDR1_DQ[52]
	AP40	DDR1_DQ[37]	DDR1_DQ[53]
	AP37	DDR1_DQ[38]	DDR1_DQ[54]
	AR37	DDR1_DQ[39]	DDR1_DQ[55]
	AT33	DDR1_DQ[40]	DDR1_DQ[56]
	AU33	DDR1_DQ[41]	DDR1_DQ[57]
	AU30	DDR1_DQ[42]	DDR1_DQ[58]
	AT30	DDR1_DQ[43]	DDR1_DQ[59]
	AR33	DDR1_DQ[44]	DDR1_DQ[60]
	AP38	DDR1_DQ[45]	DDR1_DQ[61]
	AR30	DDR1_DQ[46]	DDR1_DQ[62]
	AP30	DDR1_DQ[47]	DDR1_DQ[63]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[64]
	AT27	DDR1_DQ[49]	DDR1_DQ[65]
	AT26	DDR1_DQ[50]	DDR1_DQ[66]
	AU26	DDR1_DQ[51]	DDR1_DQ[67]
	AP27	DDR1_DQ[52]	DDR1_DQ[68]
	AN27	DDR1_DQ[53]	DDR1_DQ[69]
	AN26	DDR1_DQ[54]	DDR1_DQ[70]
	AP26	DDR1_DQ[55]	DDR1_DQ[71]
	AT22	DDR1_DQ[56]	DDR1_DQ[72]
	AU22	DDR1_DQ[57]	DDR1_DQ[73]
	AU21	DDR1_DQ[58]	DDR1_DQ[74]
	AT21	DDR1_DQ[59]	DDR1_DQ[75]
	AN22	DDR1_DQ[60]	DDR1_DQ[76]
	AP22	DDR1_DQ[61]	DDR1_DQ[77]
	AP21	DDR1_DQ[62]	DDR1_DQ[78]
	AN21	DDR1_DQ[63]	DDR1_DQ[79]




TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]



TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

Security Classification	LC Future Center Secret Data		Title	
Issued Date	2016/2/3	Deciphered Date	2015/08/10	
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Date:	Tuesday, December 20, 2016	Sheet	5	of 100



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RC113 OP, RC148 short (XDP_TDO→ PCH_TDO)
RC138 OP, RC145 short (XDP_TMS→ PCH_TMS)
RC137 OP, RC147 short (XDP_TRST→ PCH_TRST)
RC142 OP, RC143 short (XDP_TCK0→ JTAGX)
RC139 OP, RC146 short (XDP_TDI→ PCH_TDI)
```

**Primary (XDP/CMC) Debug Port**

**Kaby Lake**

TP

PROC\_TDI

PROC\_TMS

PROC\_TRSTn

PROC\_TDO

PROC\_TCK

JTAGX

PCH\_JTAG\_D0

PCH\_JTAG\_TMS

PCH\_JTAG\_TCK

PCH\_JTAG\_TDI

PCH\_TRSTn

XDP\_TRSTn

XDP\_TMS

XDP\_TCK1

XDP\_TCK0

XDP\_TDI

XDP\_TDO

R5 51 Ohm VCCSTG

R6 51 Ohm GND

EMPTY

R4 51 Ohm VCCSTG

R3 100 Ohm VCCSTG

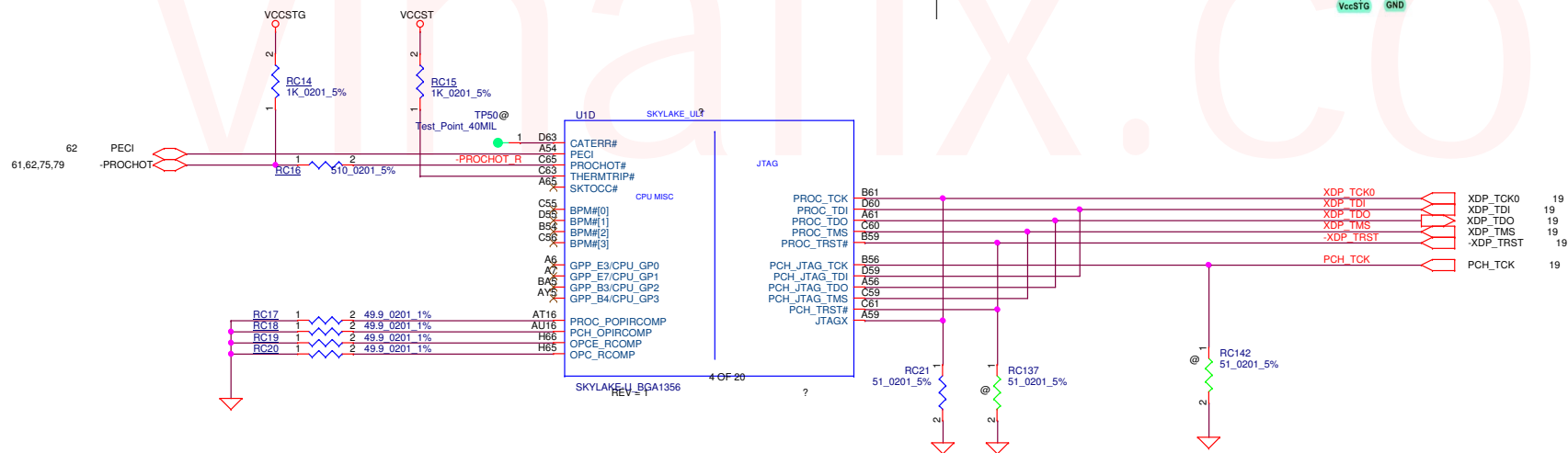
R1 100 Ohm VCCSTG



R2 51 Ohm GND

VCCSTG

GND

- Stubs on TCK1, TCK0, TMS, TDI, TDO and TRST# nets should not be more than 200ps.
- TCK0, TDI, TDO, TMS Start topology routing must be forked at within 200ps (or 1.1") from the pin.
- The Pull Up/Pull down terminations (R1, R2, R3, R4, R5, R6, R7, R8) should be placed to within 200ps of the respective Kaby Lake pins.
- TP = Test Point Pad (size - 18 mil min, 25 mil preferred)



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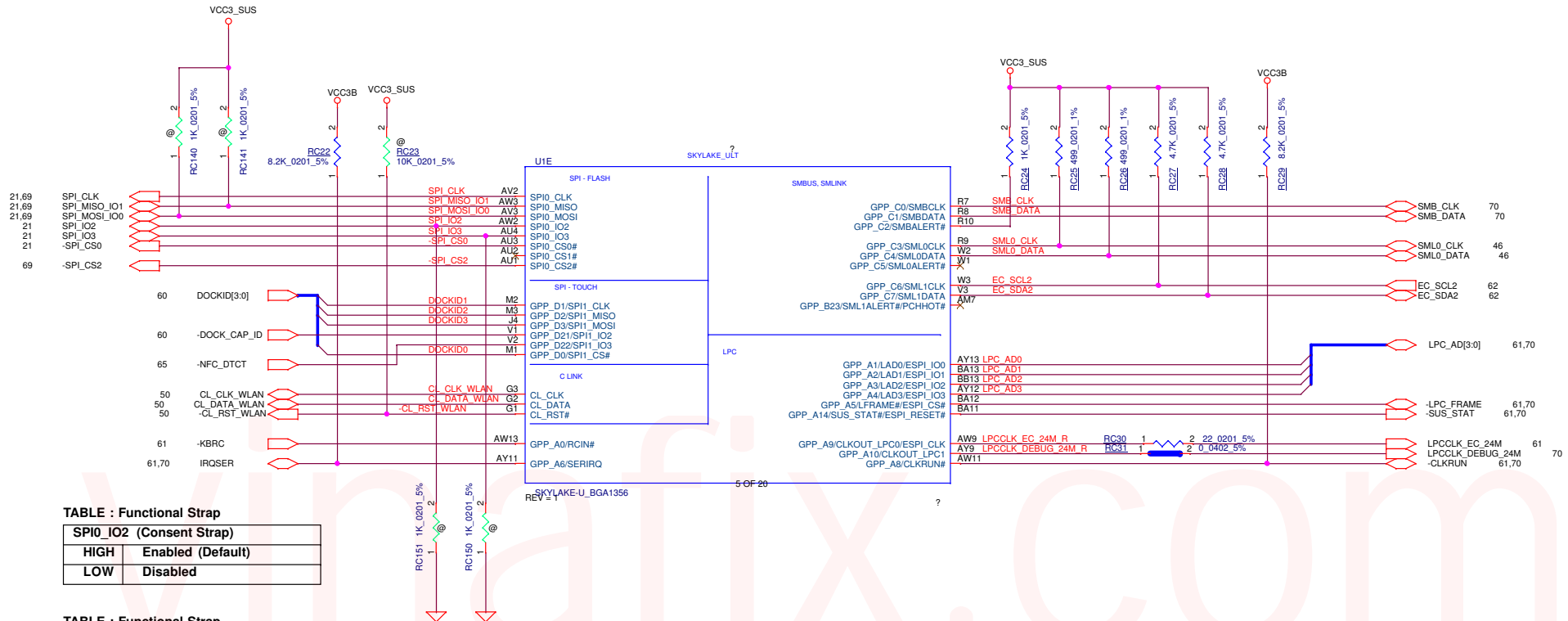


TABLE : Functional Strap

SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Functional Strap

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled

TABLE : Functional Strap

SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

TABLE : Functional Strap

SPI0_MISO (JTAG ODT Disable)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Functional Strap

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

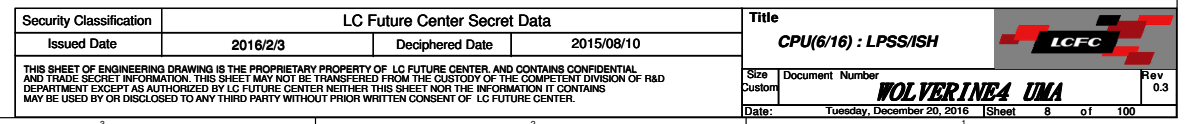
TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC

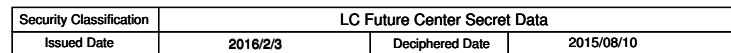
GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

GPP_B18/GPIO_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)





HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

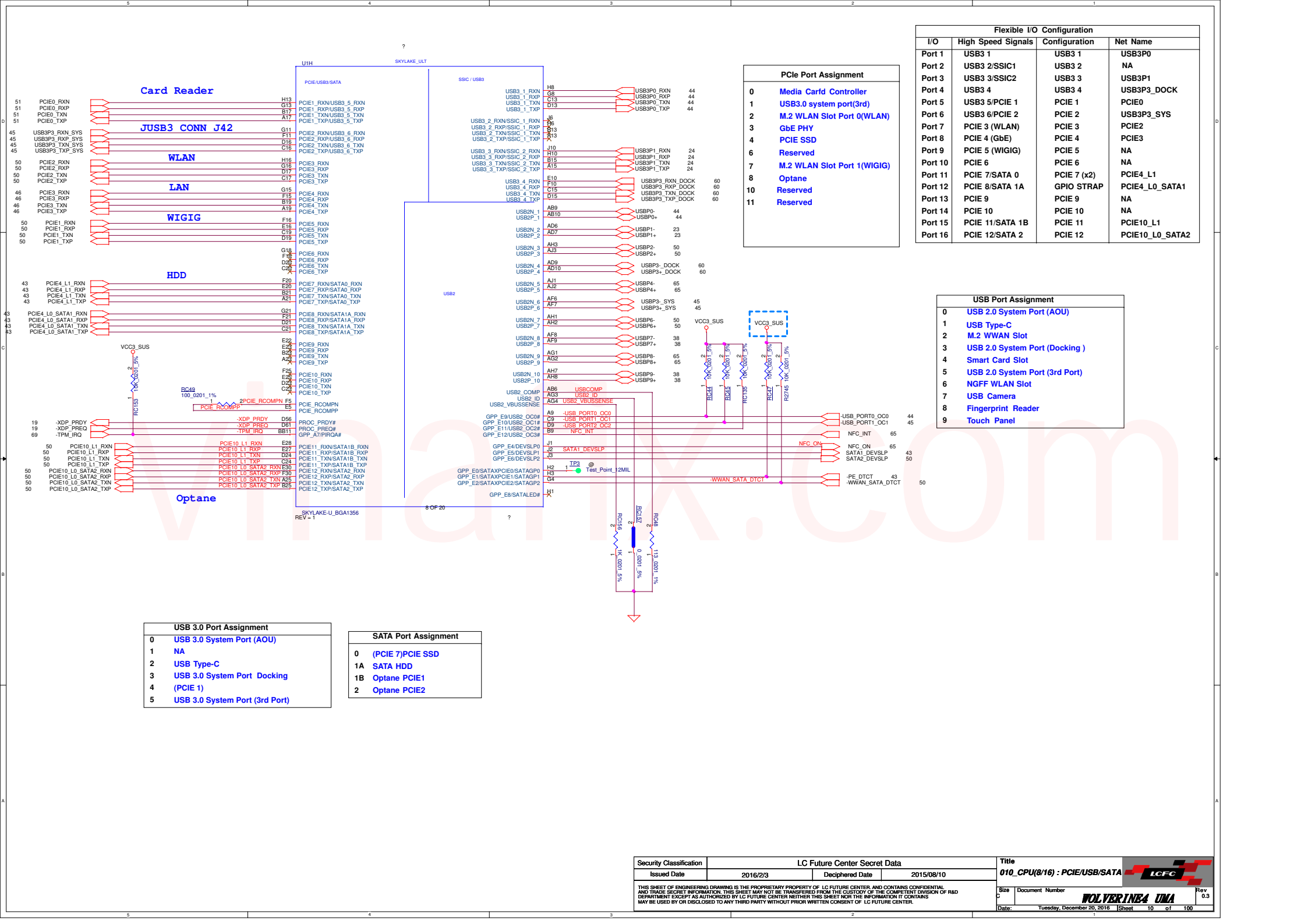


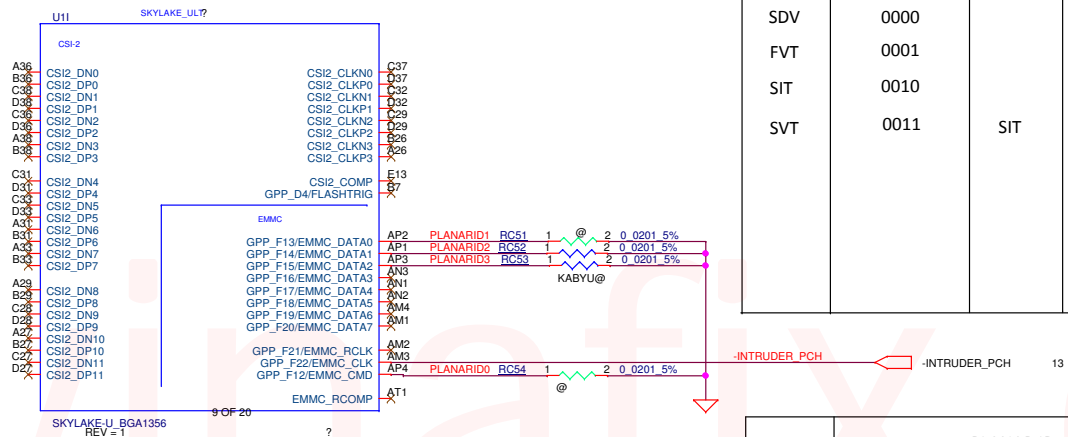
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Title	<b>CPU(7/16) : AUDIO/SDXC</b>
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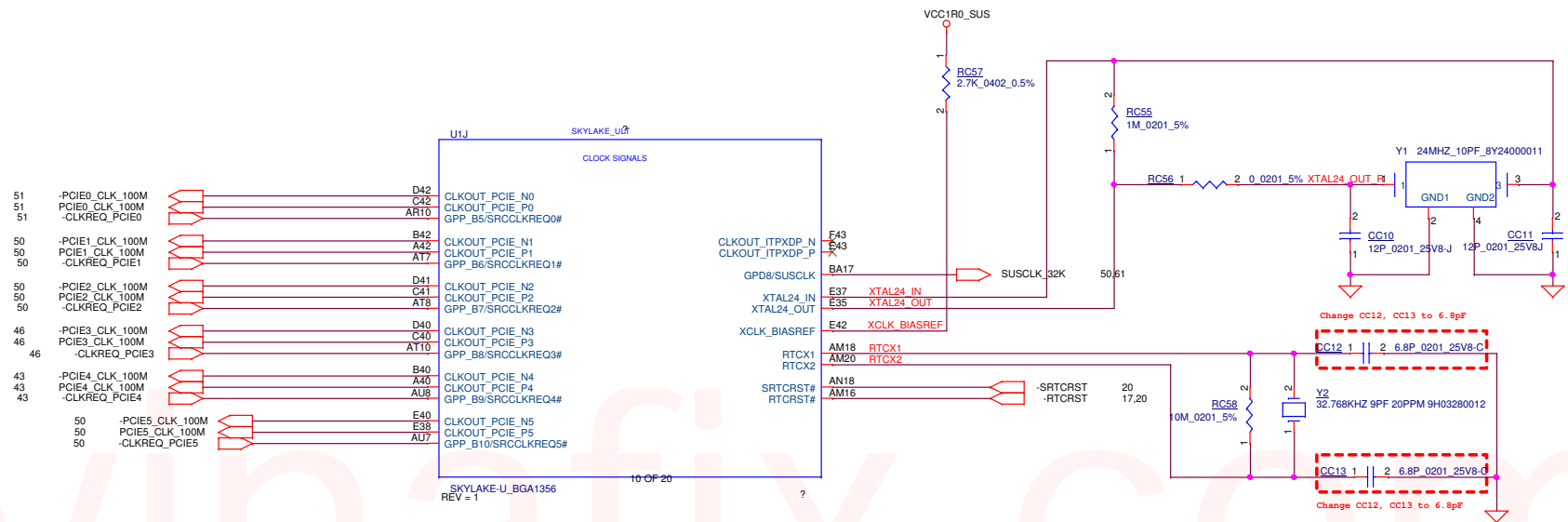
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Date:	Tuesday, December 20, 2016	Sheet 9 of 100





Kabylake	PLANAR ID[3..0]	SKYLAKE	PLANAR ID[3..0]
SDV	0000		
FVT	0001		
SIT	0010		
SVT	0011	SIT	1011

LEVEL	PLANAR ID			
	3	2	1	0
	RC53	RC52	RC51	RC54
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM



Y2 32.768KHZ

Vendor	Intel ESR spec	LCFC P/N	Vendor P/N	Vendor ESR spec
KDS	50K ohm Max	SJ100069400	1TJF090DJ1A000B	50K ohm Max
SEIKO	50K ohm Max	SJ100001X00	X1A000141000200	50K ohm Max
TXC	50K ohm Max	SJ10000J900	9H3280012	50K ohm Max

Y1 24MHZ

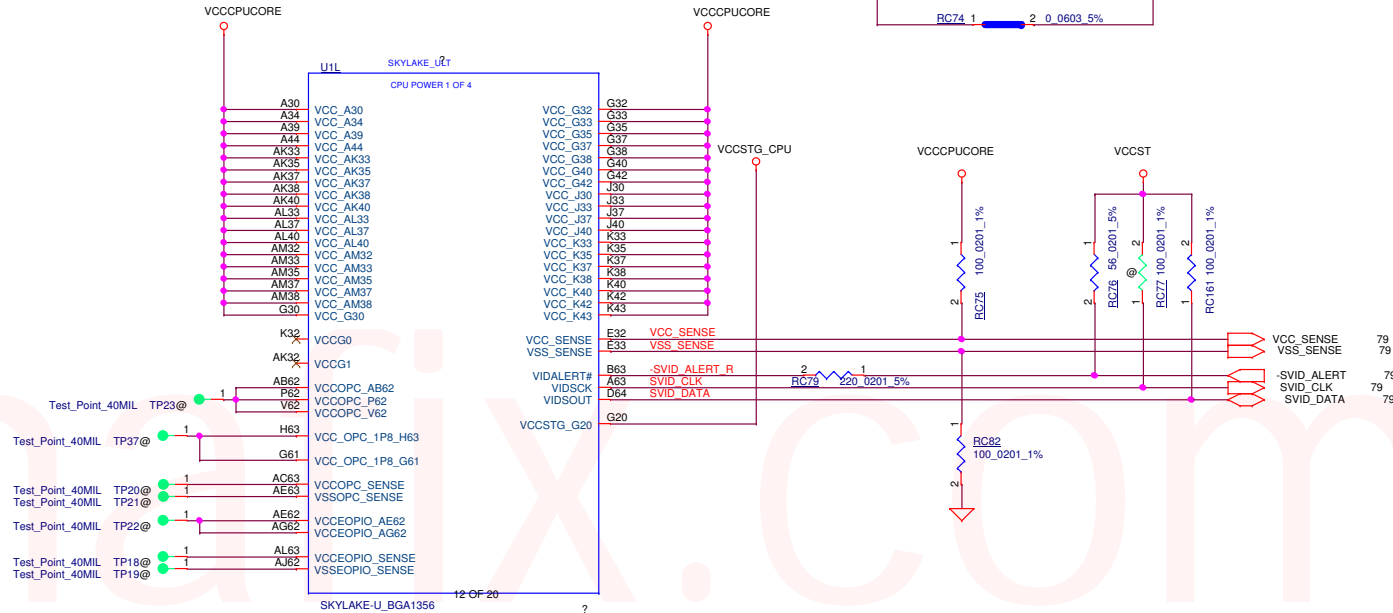
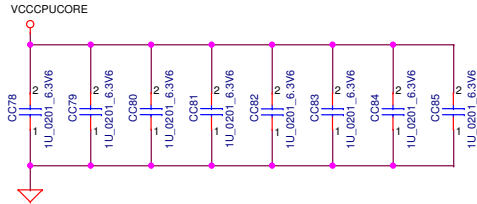
Vendor	Intel ESR spec	LCFC P/N	Vendor P/N	Vendor ESR spec
TXC	50 ohm Max	SJ10000HH0J	8Y24000011	50 ohm Max
KDS	50 ohm Max	SJ10000P100	1ZZHAE24000BC0D	50 ohm Max

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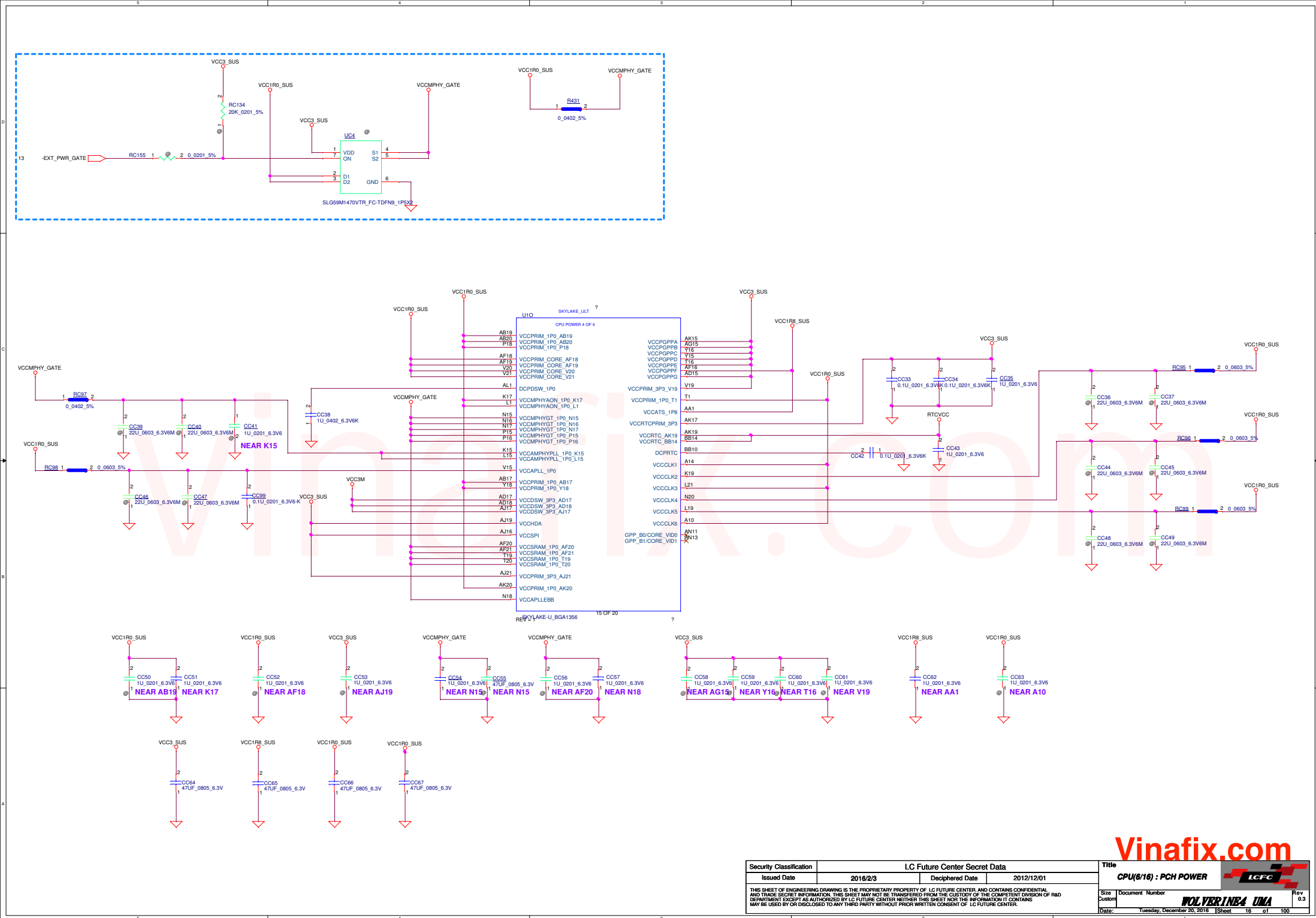






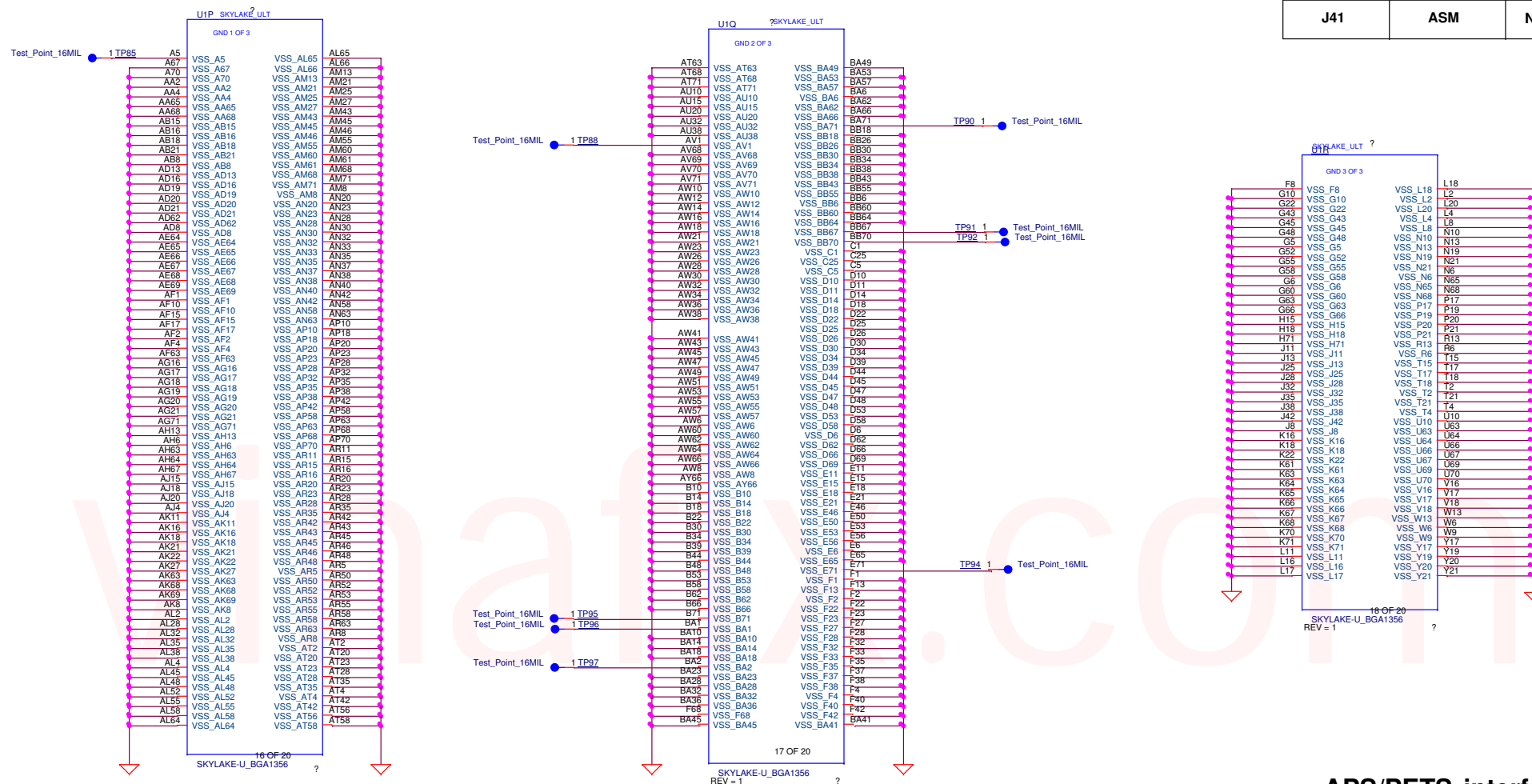




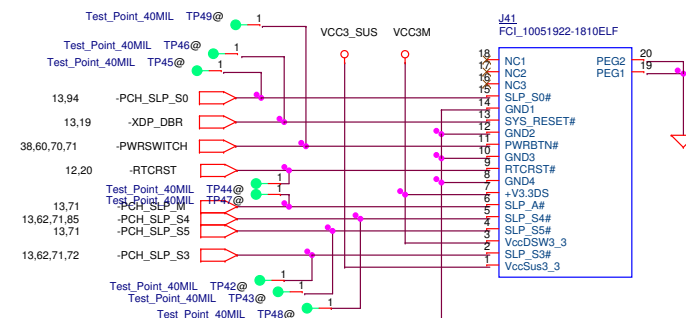




CONNECTOR	Planar Only	BOX
J41	ASM	NO ASM



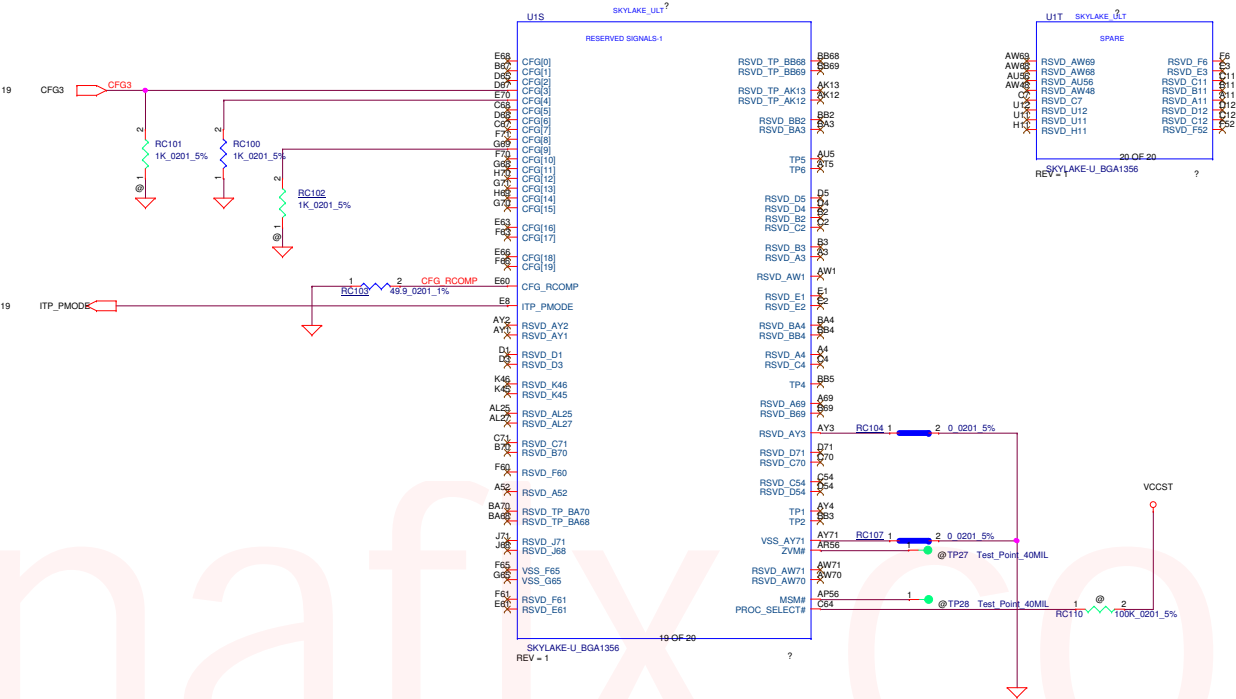
## APS/PETS interface



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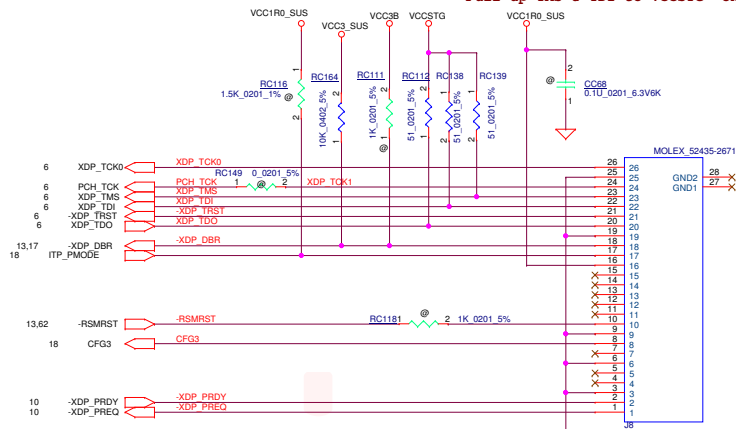
TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled



-XDP\_DBR Pull Up 10k to VCC3\_SUS on 2016/3/17

Pull up TMS & TDI to VCCSTG on 2016/3/11



### TABLE: CPU ITP DEBUG PORT

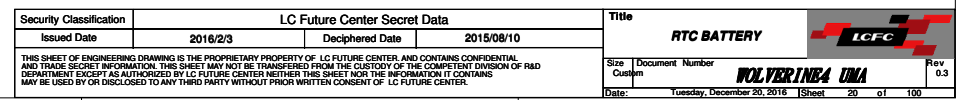
SIGNAL	REF DES	Planar only	BOX
TDO	RC109	ASM	ASM
TRST#	RC113	ASM	ASM
DBRST#	RC110	ASM	ASM
RESET#	RC111	ASM	ASM
PWRGD	RC112	ASM	ASM
CONNECTOR	J8	ASM	NO ASM

**NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV**

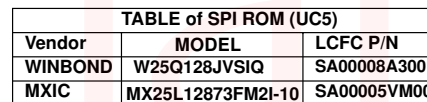
**TABLE: PCH ITP DEBUG port**

SIGNAL	REF DES	Planar only	BOX
TDO	RC114	ASM	ASM
TMS	RC116	ASM	ASM
TDI	RC115	ASM	ASM
TCK	RC117	ASM	ASM
CPUCORE_PWRGD	RC118	ASM	ASM
-RSMRST	RC119	ASM	ASM
CONNECTOR	J9	ASM	NO ASM

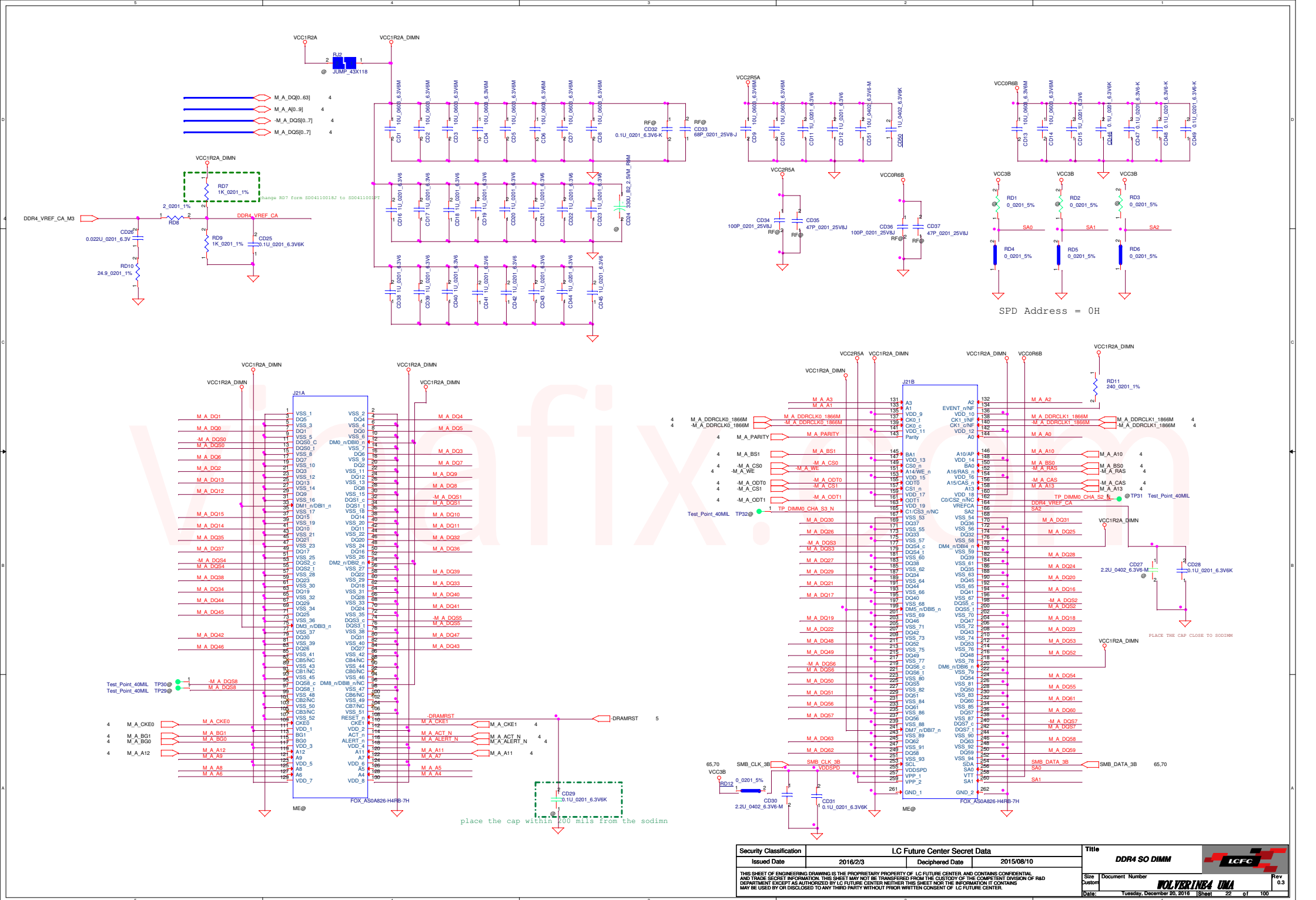
**NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV**

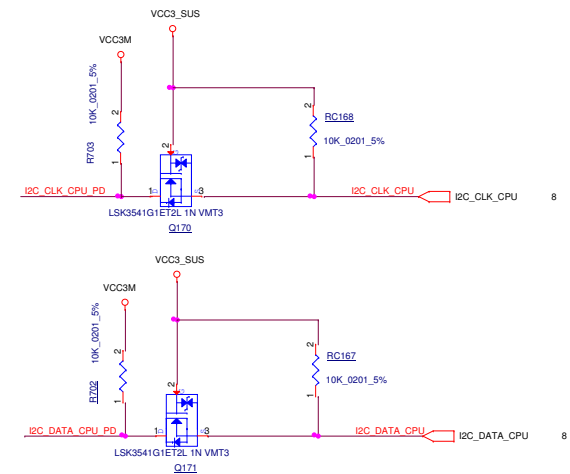




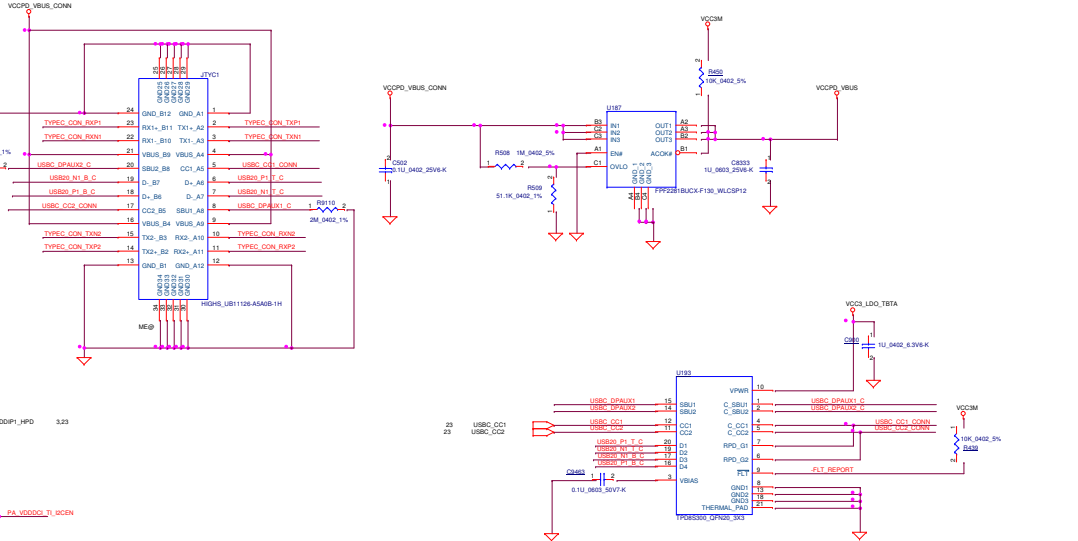


SF100 PIN HEADER INTERFACE (TOP VIEW)					
1	VCC	DC4.1	GND	GND	2
3	CS#	RC128.2	RC129.2	CLK	4
5	MISO	RC132.2	RC130.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8





Title		MUX & PD			
Size	Document Number	<b><i>WOLVERINE4 UMA</i></b>			Rev 0.3
Date:	Tuesday, December 20, 2016, 13:50:23 of 100				




Module Configuration for PS8743 Mode Selection						
State #	CE DP Pin32 (CTL1)		CE USB Pin35 (CTL6)		FLIP Pin38 (FLIP)	MODE
0 <td>H</td> <td>H</td> <td>H</td> <td>H</td> <td></td> <td>1-port USB on SS2 2-lane DP . DP ML0 is on SSRX1(Flipped)</td>	H	H	H	H		1-port USB on SS2 2-lane DP . DP ML0 is on SSRX1(Flipped)
1	H	H	H	L		1-port USB on SS1 2-lane DP . DP ML0 is on SSRX2(Un-flipped)
2	H	L	L	H		4-lane DP . DP ML0 is on SSRX1(Flipped)
3	H	L	L	L		4-lane DP . DP ML0 is on SSRX2(Un-flipped)
4	L	L	H	H		1-port USB only on SS2 channels (Flipped)
5	L	L	H	L		1-port USB only on SS1 channels (Un-flipped)
6	L	L	L	H		Chip power down
7	L	L	L	L		Chip power down

[illegible]




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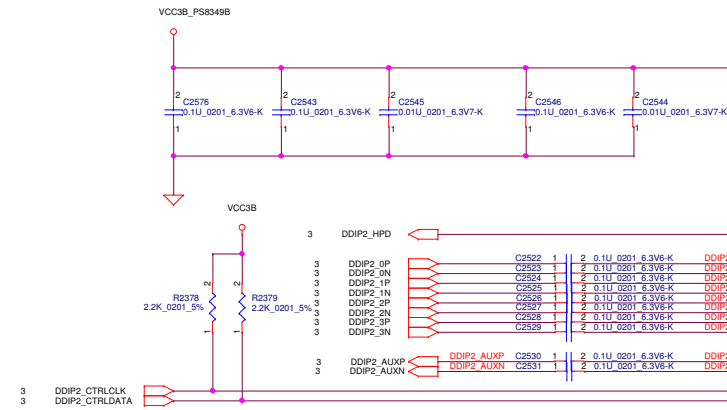
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				Rev	0.3





R2378 and R2379 unmounted, although U147 PU internally

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI\_PRIORITY2)

Port 1 has higher priority when both ports are plugged

Port 2 has higher priority when both ports are plugged

Follow thorpe priority setting

**PRIORITY : DOCKING>HDMI>WIGIG**

TABLE:

SW1	SW0	Port Priority Sequence
L	L	DP1 Port > DP2 Port > TMDS Port
L	H	DP1 Port > TMDS Port > DP2 Port
H	L	TMDS Port > DP2 Port > DP1 Port
H	H	TMDS Port > DP1 Port > DP2 Port

← DEFAULT

MODE =

H : Automatic Switching mode, HDMI ID Enabled

L : Automatic Switching mode, HDMI ID Disabled

← DEFAULT




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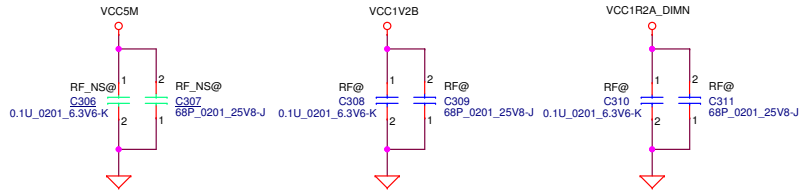
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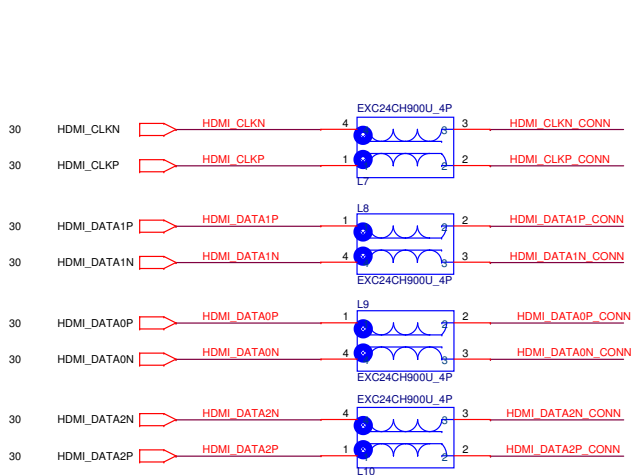
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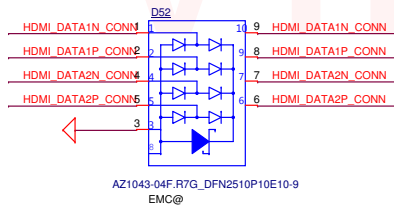
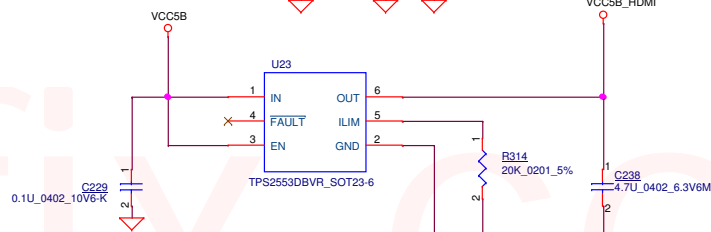
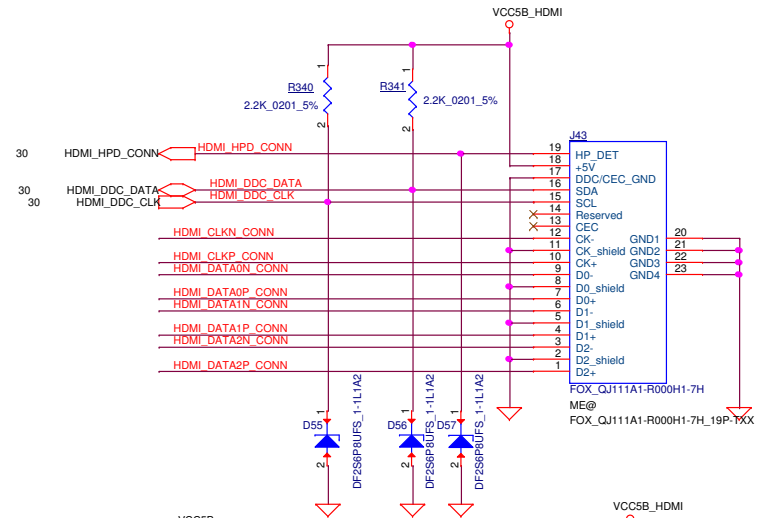
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				Custom		<b><i>WOLVERINE4 UMA</i></b>		0.3	
Date:				Tuesday, December 20, 2016		Sheet		39 of 100	

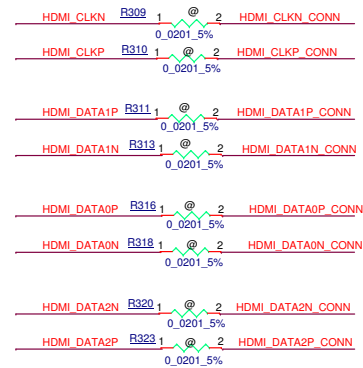
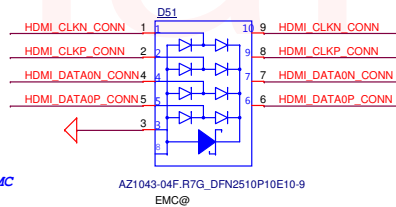


For PARADE Debug use.

HDMI_CLKN_CONN	R9121	1	2	180_0402_1%	HDMI_CLKP_CONN
HDMI_DATA1N_CONN	R9123	1	2	180_0402_1%	HDMI_DATA1P_CONN
HDMI_DATA0N_CONN	R9125	1	2	180_0402_1%	HDMI_DATA0P_CONN
HDMI_DATA2N_CONN	R9127	1	2	180_0402_1%	HDMI_DATA2P_CONN



For EMC




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Date	Tuesday, December 20, 2016	Sheet	40 of 100


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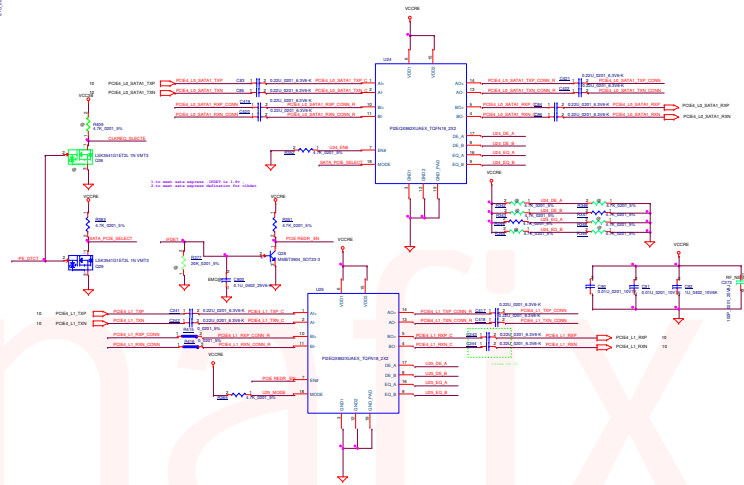
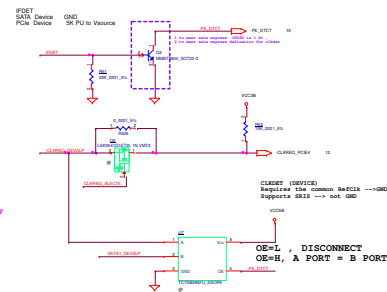
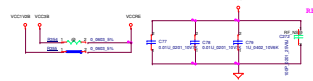
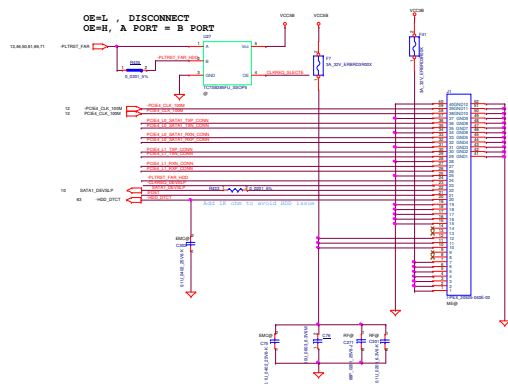
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				Date:	Tuesday, December 20, 2016	Sheet 42 of 100





Mode Configuration Table

EN5	MODE	MODE
0	0	SATA Application
0	1	PCIe Application
1	X	Double

Equalization Setting:  
EQ\_2,3 are for selection pins for the equalization selection for each direction.

Equalizer setting

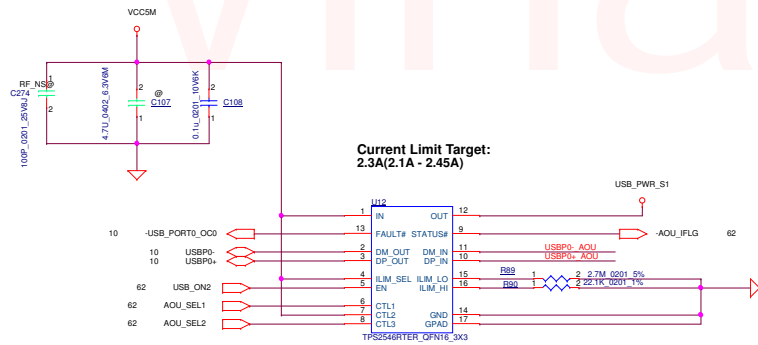
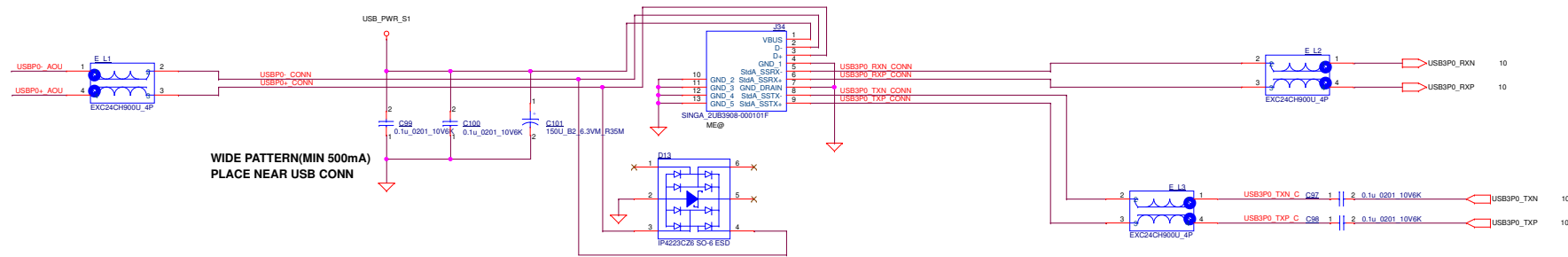
EQ_2,3	A/B	@4Gbps	@8Gbps
0	0dB	0dB	0dB
open	0dB (default)	0dB (default)	0dB (default)
1	0dB	0dB	11dB

De-Emphasis Setting (for PCIe only):

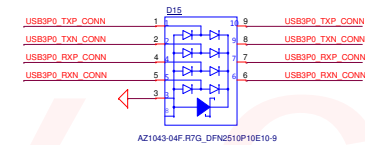
Output DE-Emphasis Setting

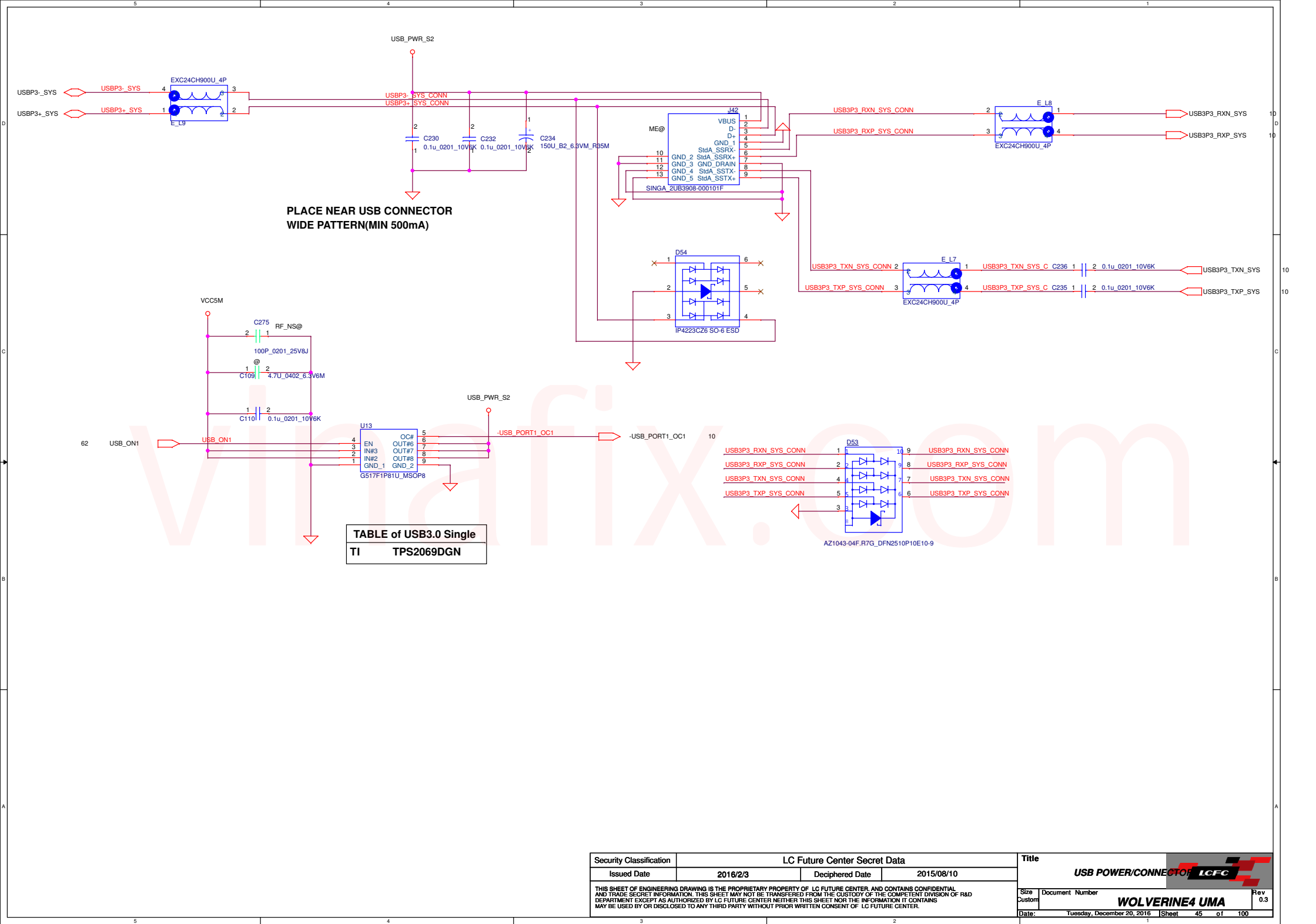
DE	DE Emphasis
0	1.5 dB
open	0dB (Default)
1	4dB





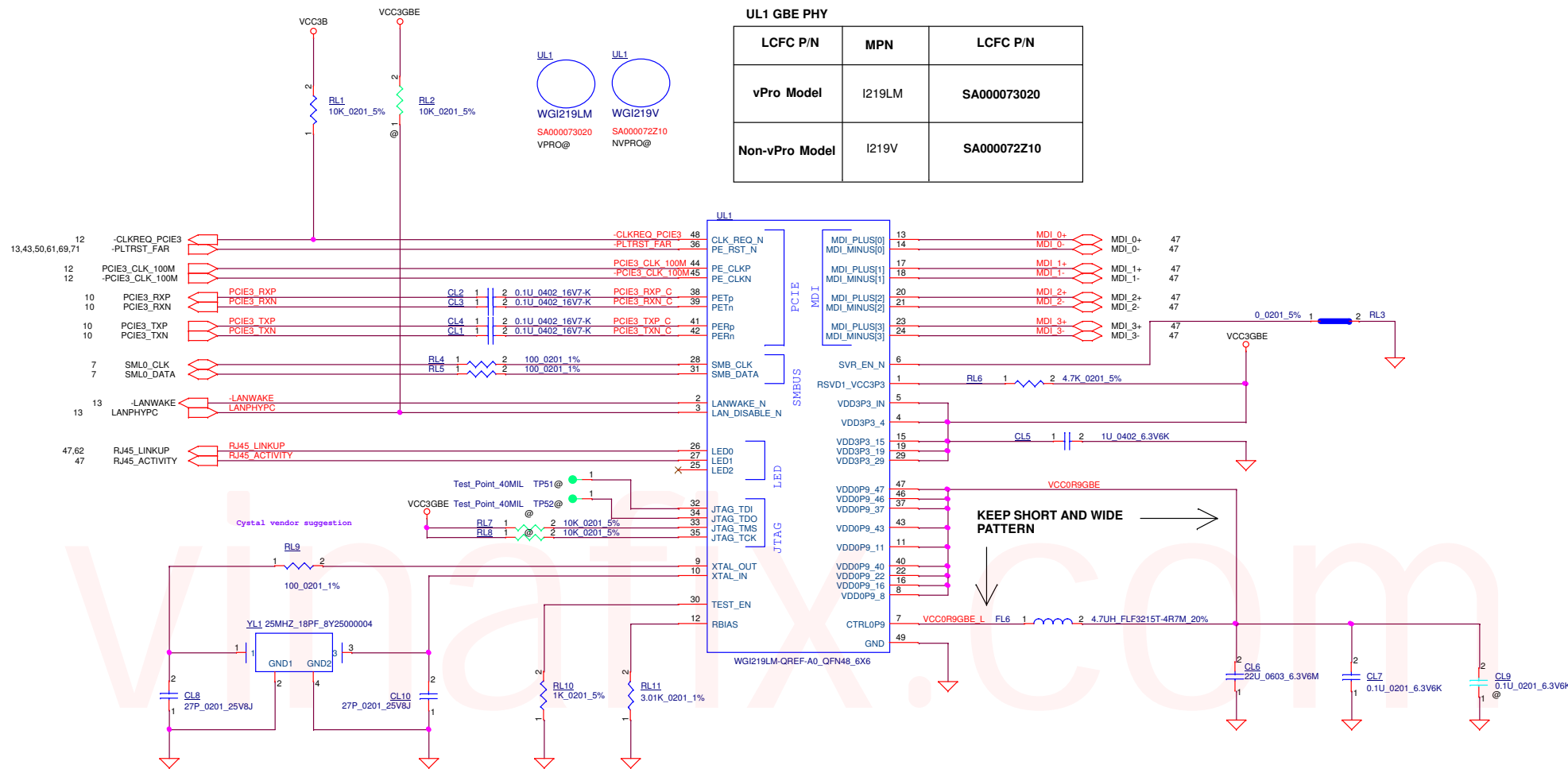
Vendor	P/N
TI	TPS2546RTER





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Title				USB POWER/CONNECTOR			
Size				Document Number			
Custom				WOLVERINE4 UMA			
Date				Tuesday, December 20, 2016			
				Sheet 45 of 100			
				Rev 0.3			



YL1 25Mhz

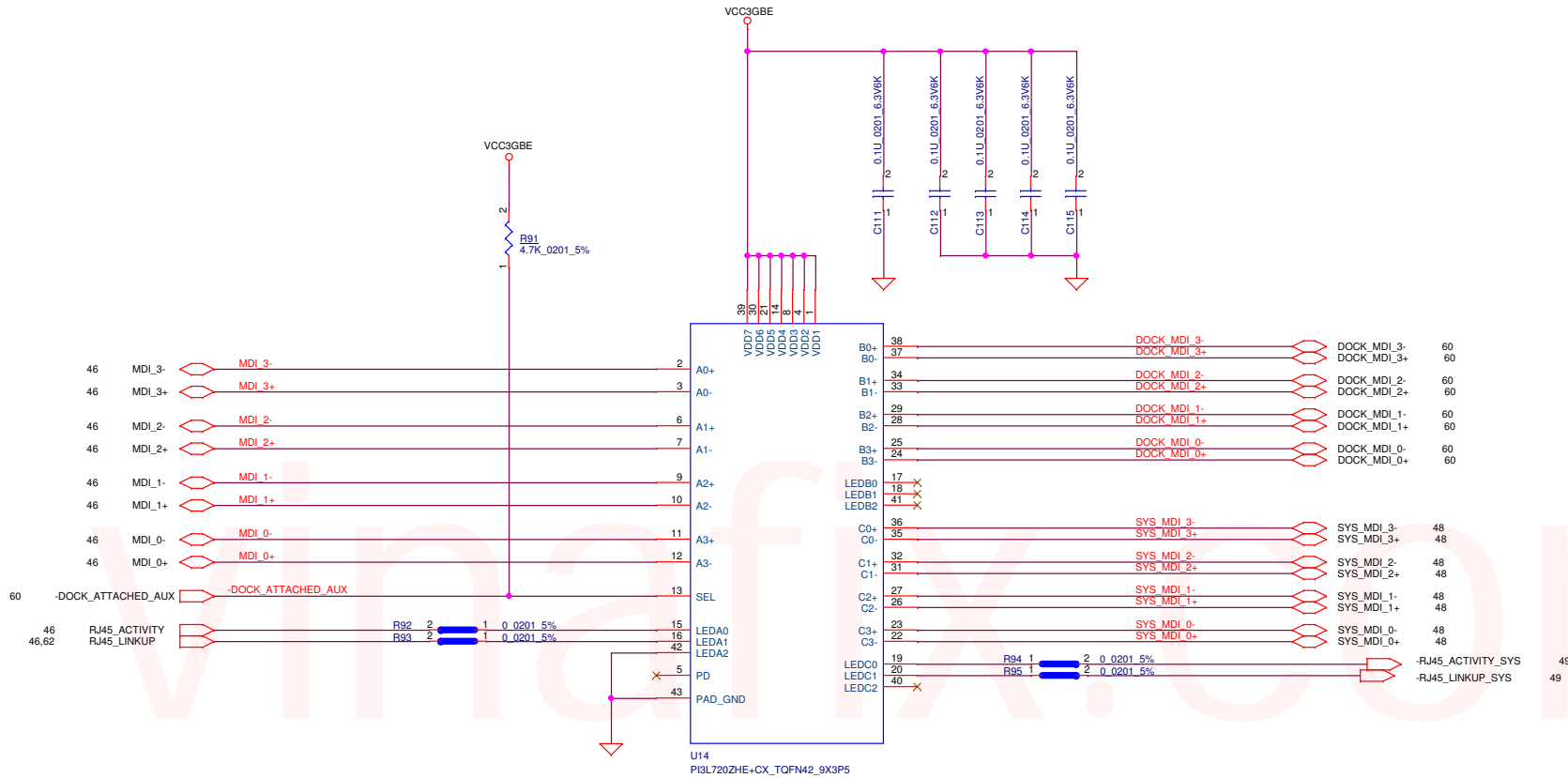
Vendor	Intel ESR spec	LCFC P/N	Vendor P/N	Vendor ESR spec
TXC	50 ohm Max	SJ10000H00J	8Y25000004	50 ohm Max
KDS	50 ohm Max	SJ10000P300	1ZZHAE25000CC0F	50 ohm Max

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U14 GBE LAN SWITCH TABLE

LCFC P/N	VENDOR	MPN
SA00007E900	PERICOM	PI3L720ZHE+CX
SA000072400	TI	TS3L501ERUAR

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Title		Rev	
GBE LAN SWITCH		0.3	
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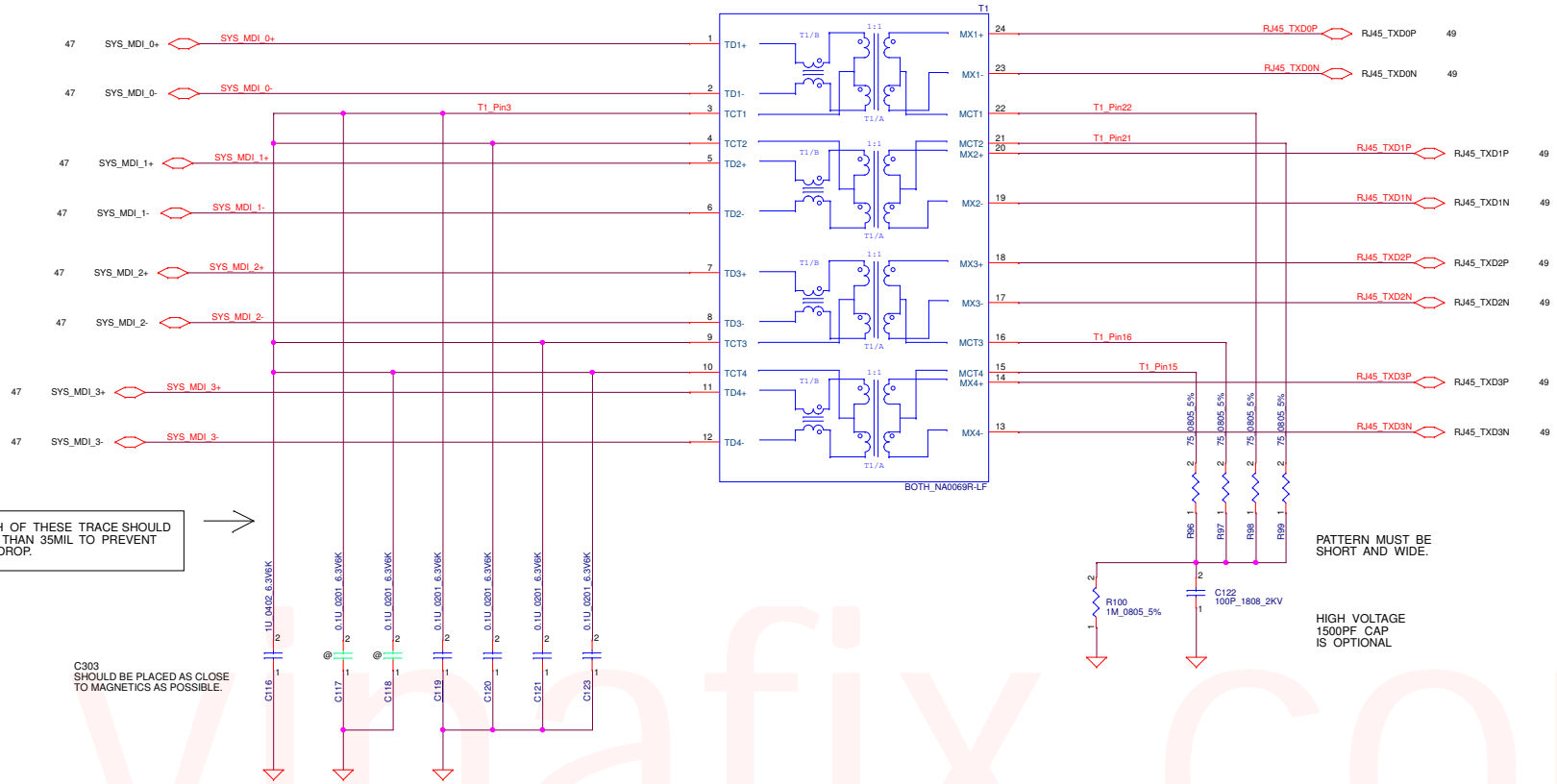
**VOLVERINE4 UMA**

THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

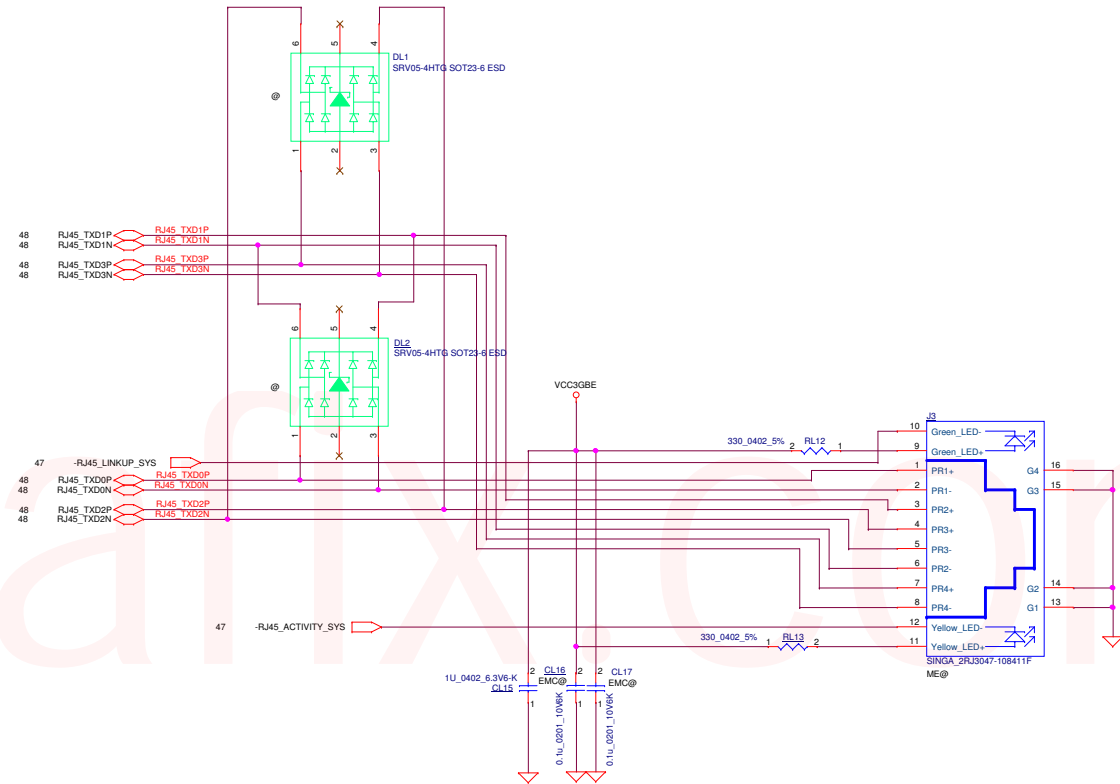
C303 SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.


ESD REASON

Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF

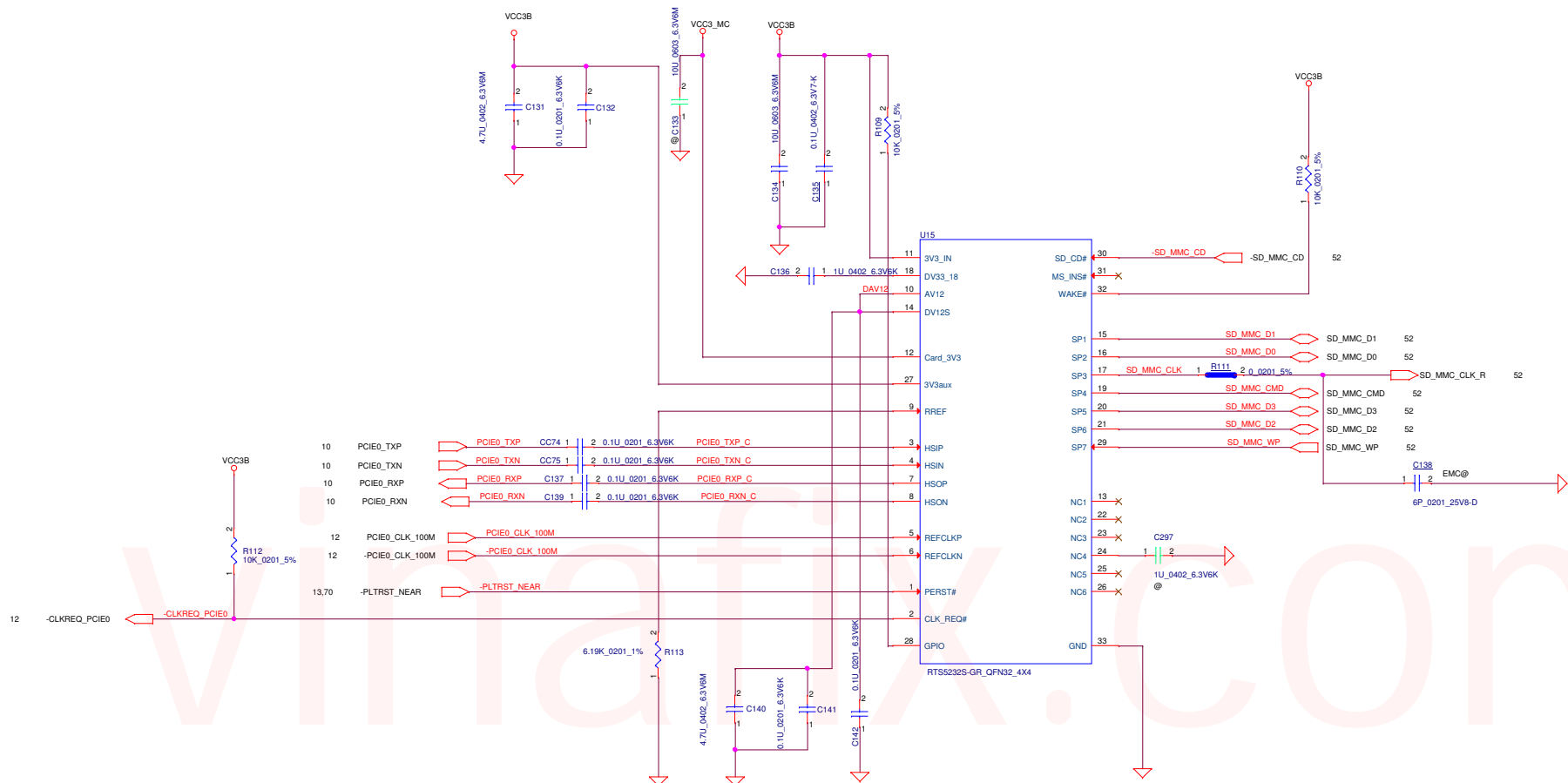


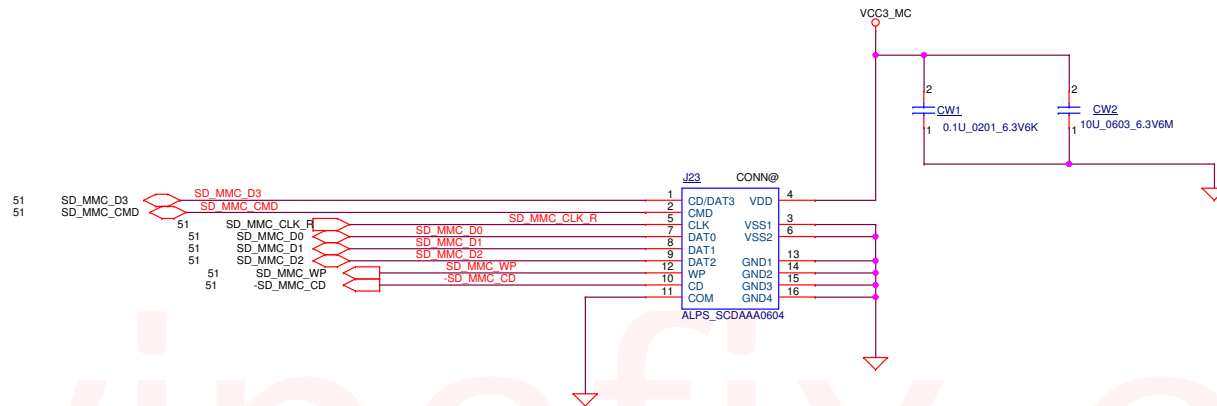




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				Sheet 52	of 100

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Security Classification	LC Future Center Secret Data			Title	
Issued Date	2016/2/3	Deciphered Date	2015/08/10	SMART CARD I/F	
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Size		Document Number		Rev	
Custom		WOLVERINE4 UMA		0.3	
Date:		Tuesday, December 20, 2016		Sheet 53 of 100	

TABLE

Dock support		
	SUPPORT	NON-SUPPORT
R1235	NO ASM	NO ASM
R1236	ASM	NO ASM
R1237	ASM	NO ASM
R1238	ASM	NO ASM

↑  
**LOGIC**

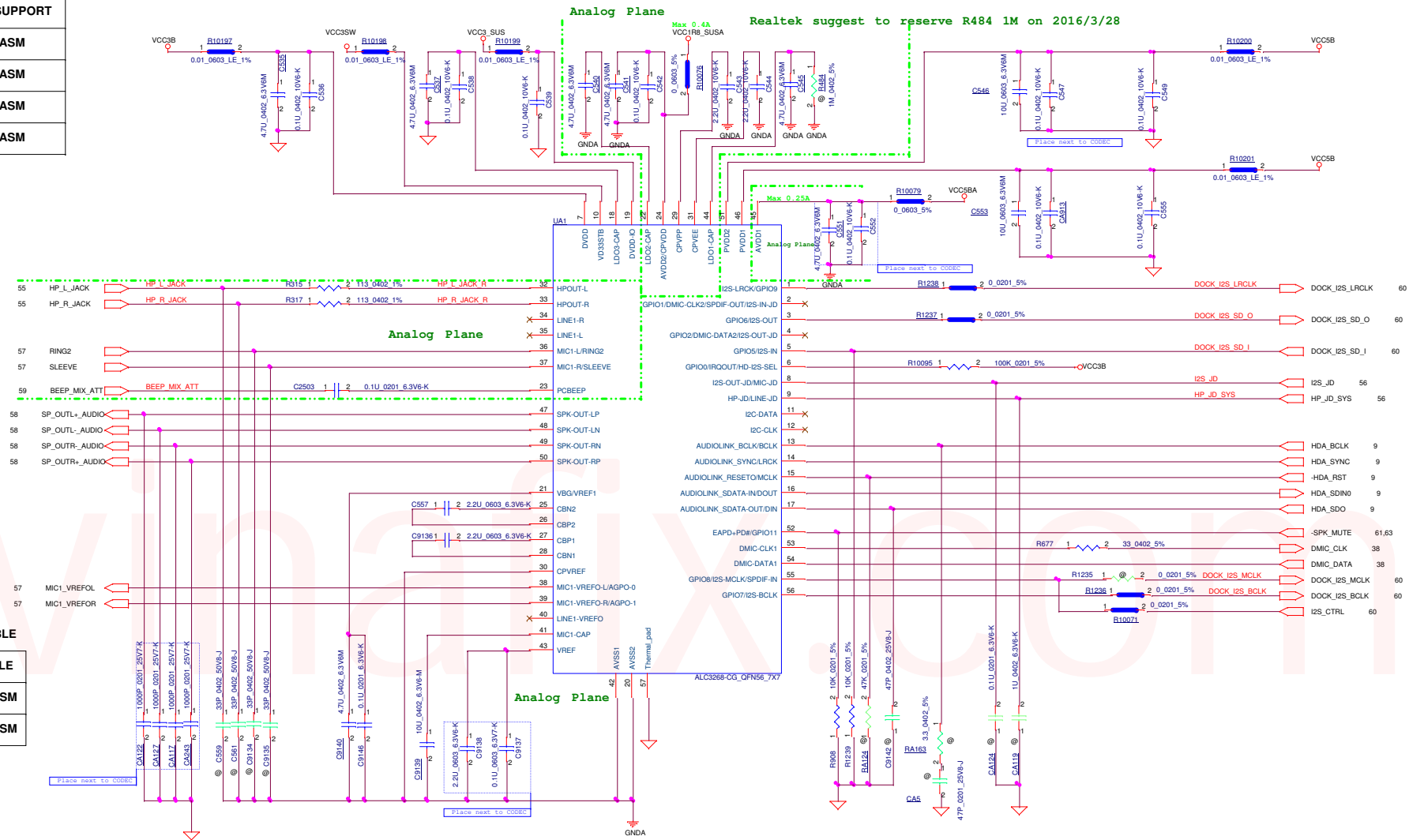
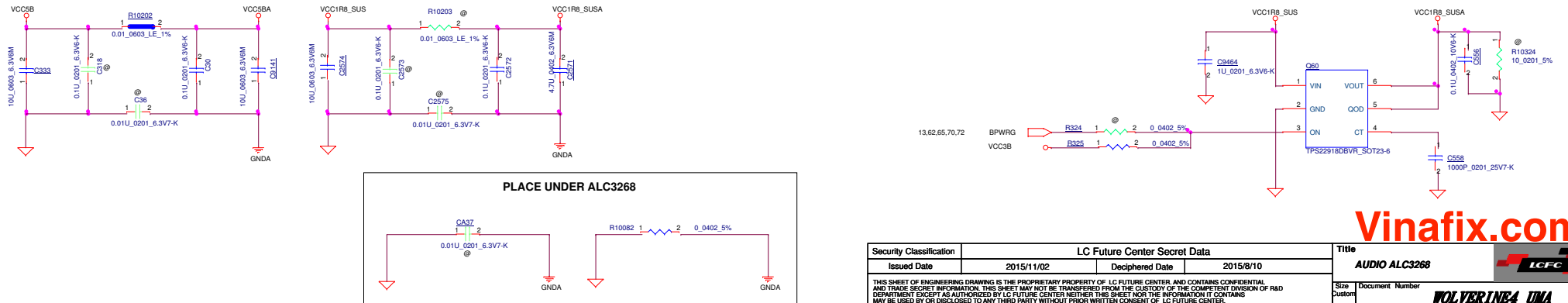


TABLE	MIC HW ENABLE/DISABLE
-------	-----------------------



	ENABLE	DISABLE
R961	ASM	NO ASM
R677	ASM	NO ASM

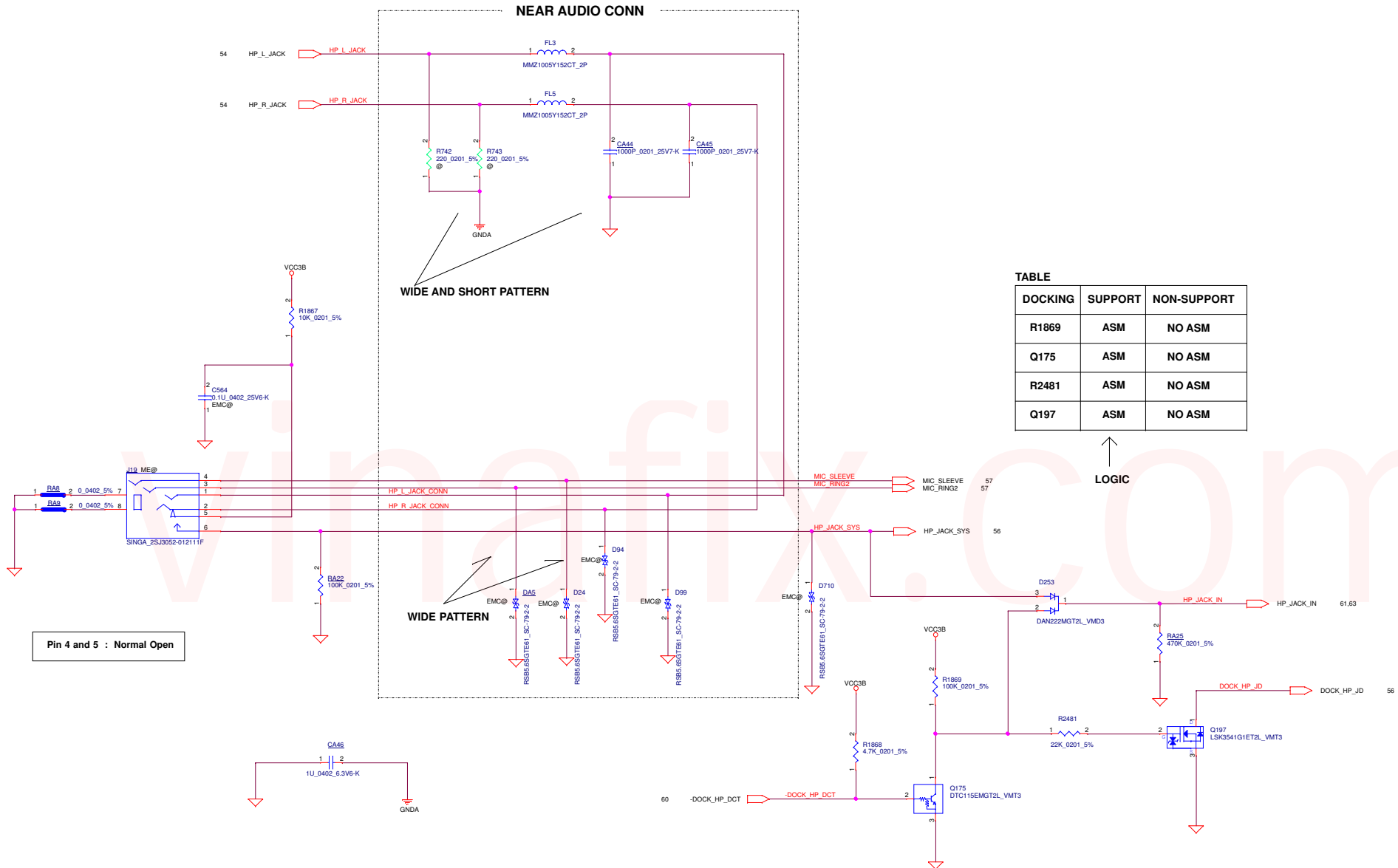
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**LOGIC**



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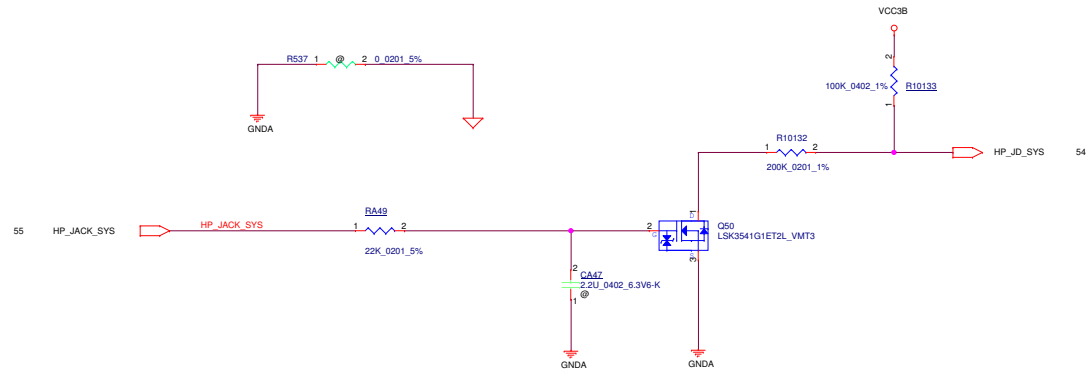


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Issued Date	2015/11/02	Deciphered Date	2015/8/10			
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				Date:	Tuesday, December 29, 2016 15:46	
					USA	100



DOCKING	SUPPORT	NON-SUPPORT
R1869	ASM	NO ASM
Q175	ASM	NO ASM
R2481	ASM	NO ASM
Q197	ASM	NO ASM

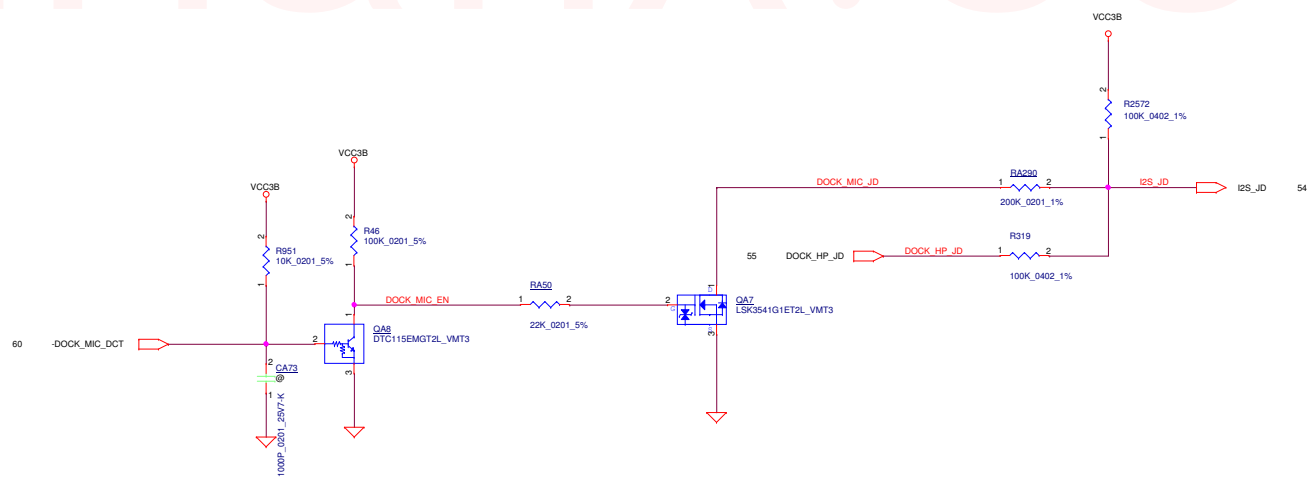
LOGIC



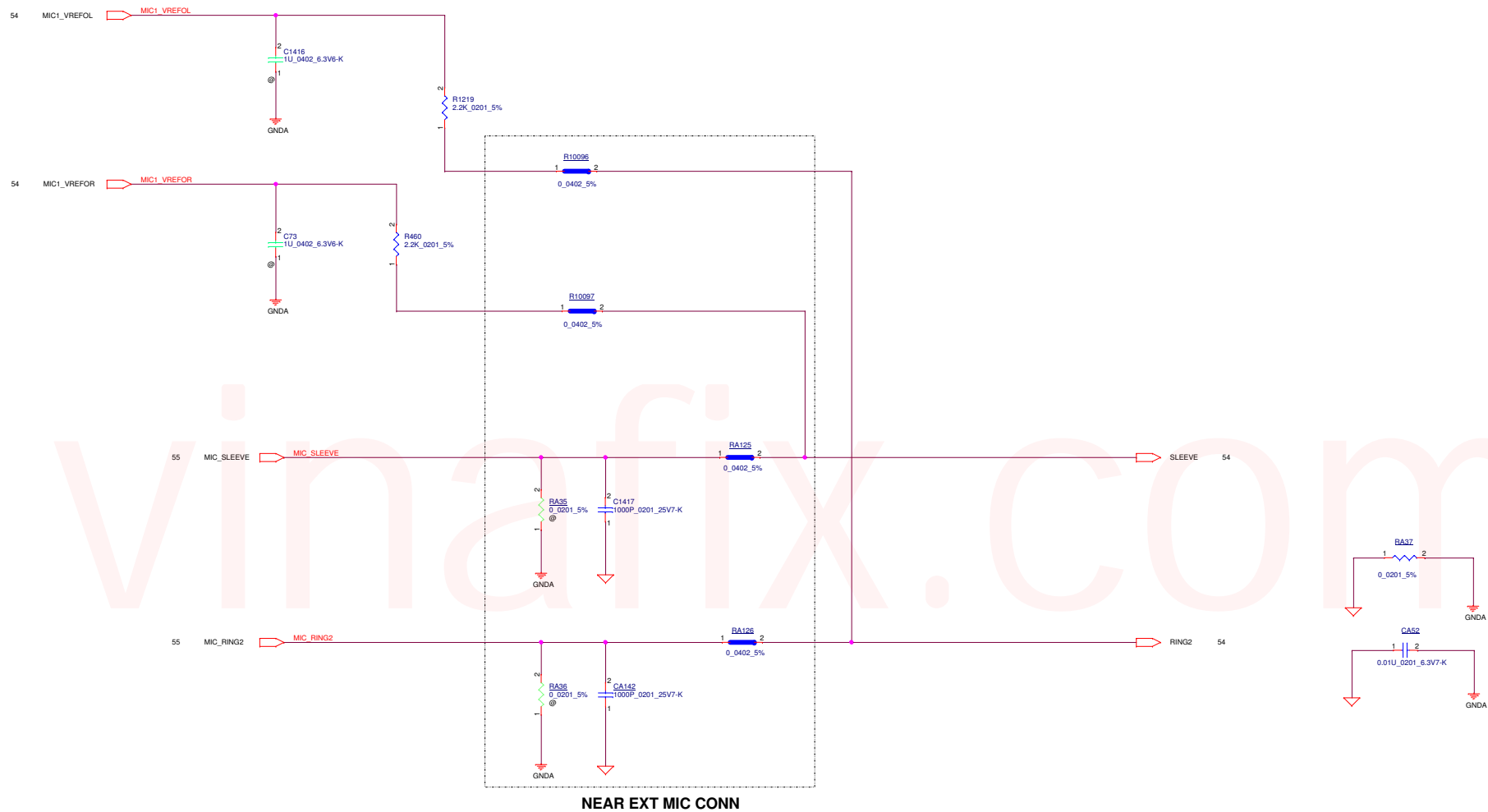
TABLE


DOCKING	SUPPORT		NON SUPPORT
	MIC HW	ENABLE	DISABLE
R951	ASM	NO ASM	NO ASM
R290	ASM	NO ASM	NO ASM
R46	ASM	NO ASM	NO ASM
Q5	ASM	NO ASM	NO ASM
R52	ASM	NO ASM	NO ASM
Q6	ASM	NO ASM	NO ASM
R319	ASM	ASM	NO ASM
R2572	ASM	ASM	NO ASM

↑  
LOGIC



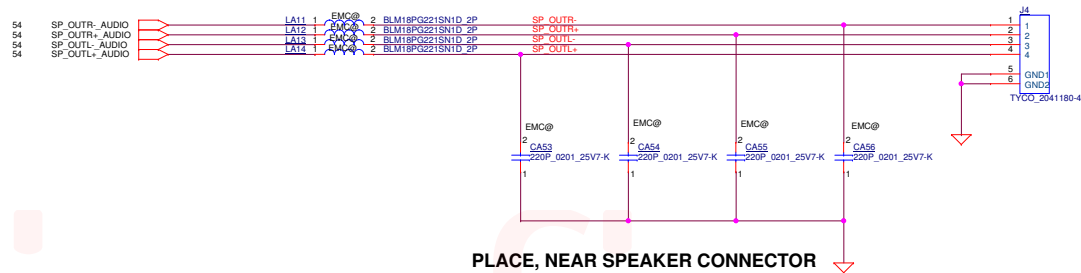




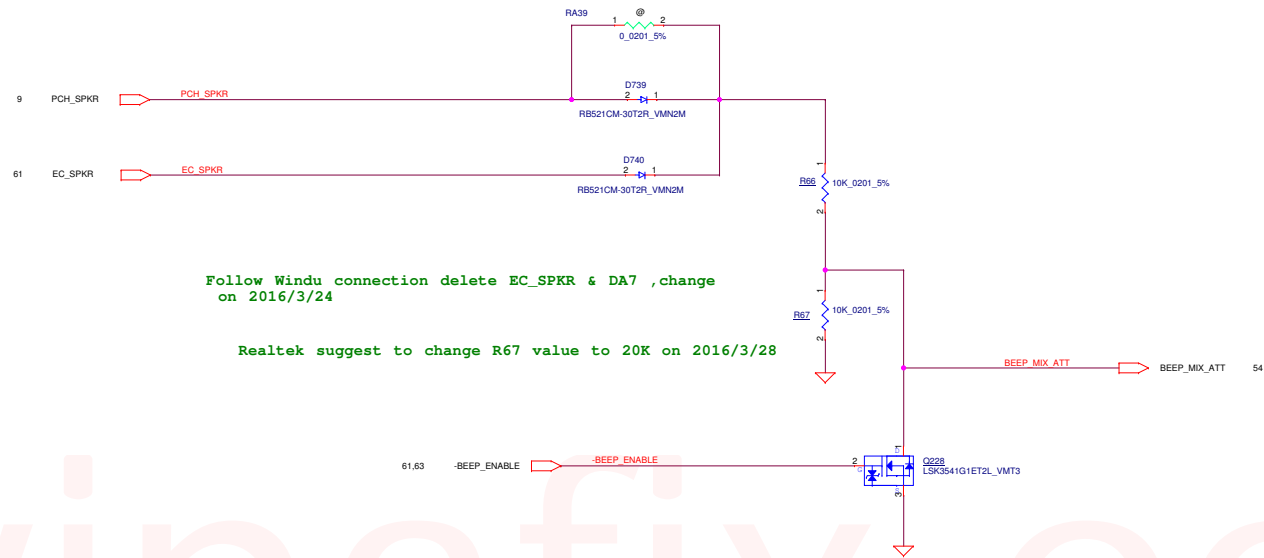
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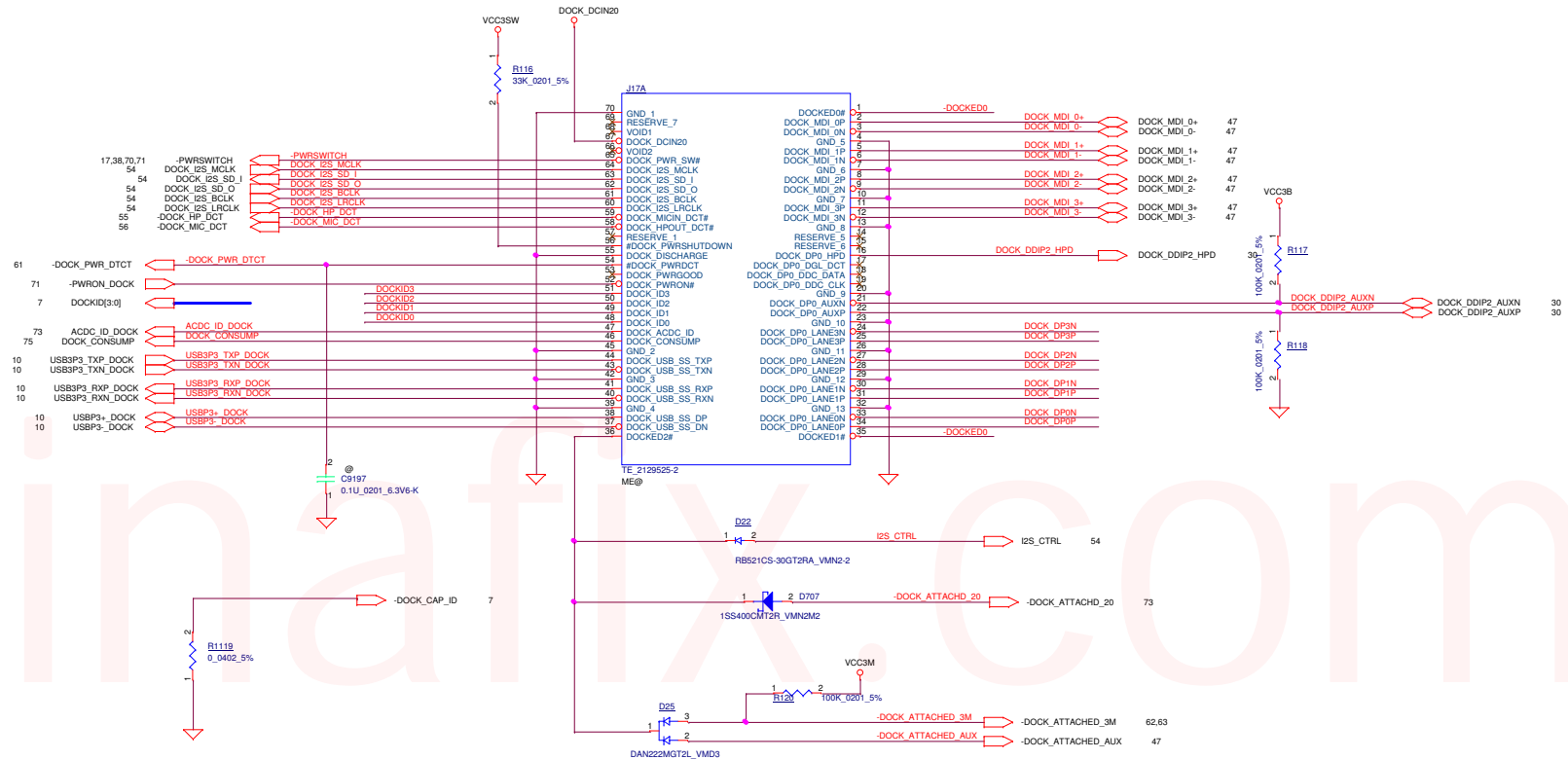
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Custom	C			0.3	
Date:	Tuesday, December 30, 2015			Sheet	59 of 100

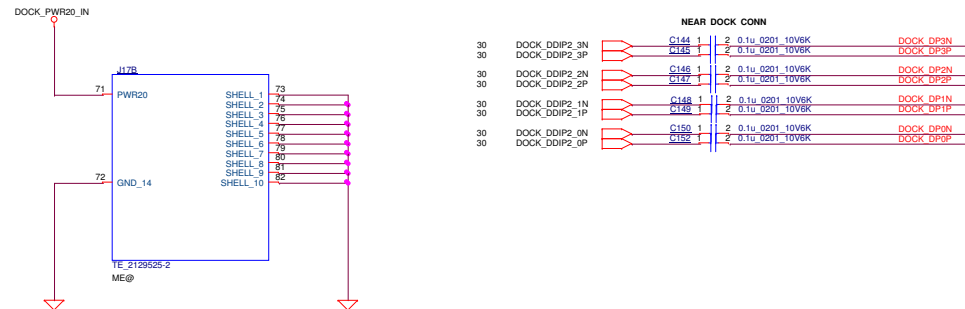


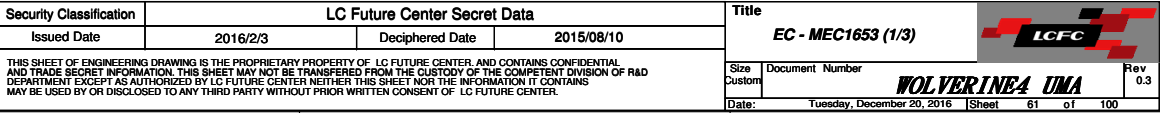
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Custom	C	0.3					
Date:	Tuesday, December 30, 2015	Sheet	59	61	100		



20160222 change to reserved to avoid duplicated DOCK\_PWR20\_IN

Q6 & D23 delete on 2016/3/17, DOCK\_PWR20\_IN power rail provided form PWR page







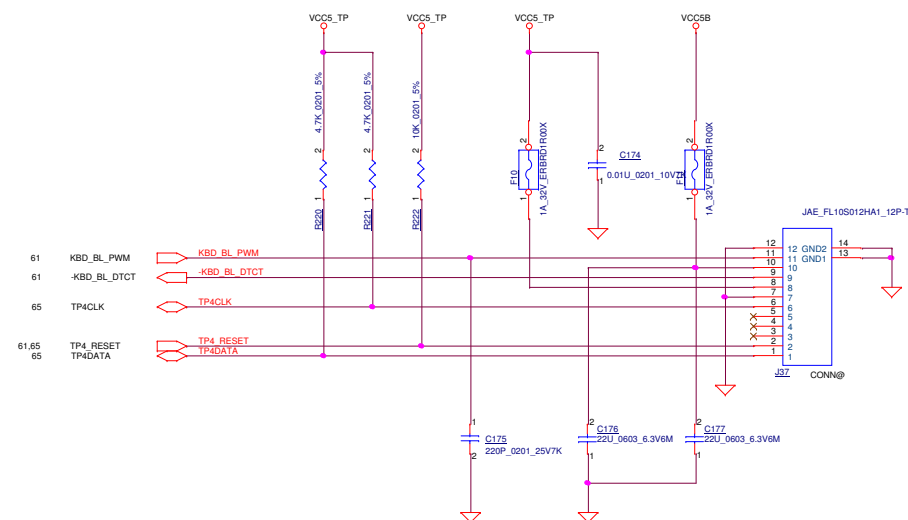
Sensor	Device	Placed on
C161+Q9	CPU DC/DC(PU402)	BOTTOM
C164+Q11	DIMM (J21)	BOTTOM
C167+Q13	WLAN (J32)	BOTTOM
C255+Q25	FAN module	TOP
C163+Q10	Charger (PU101)	BOTTOM
C166+Q12	WWAN(J22)	BOTTOM



# JTAG Pin Connection

JTAG Pin Number	Net Name
Pin1	-DOCK_ATTACHED_3M(TP11)
Pin2	BDC_ON(TP7)
Pin3	-WWAN_DISABLE(TP12)
Pin4	-WLAN_RF_KILL(TP6)
Pin5	GND
Pin6	VCC3M
Pin7	GND
Pin8	GND

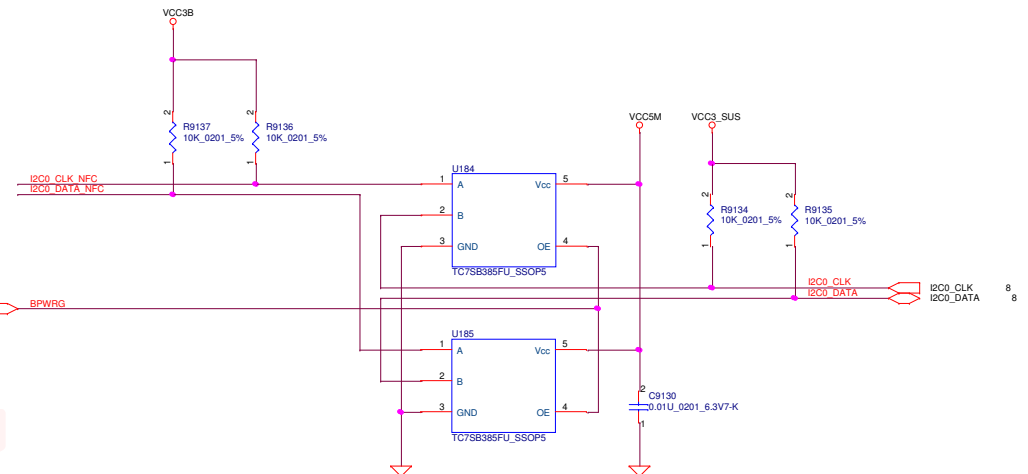
## JTAG Debug Port

	Enable	Disable
R181	ASM	NO_ASM
R182	NO_ASM	ASM
R206	ASM	NO_ASM
R209	ASM	NO_ASM
R210	ASM	NO_ASM
R211	ASM	NO_ASM

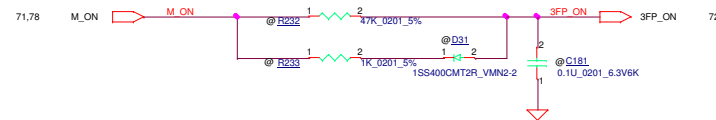
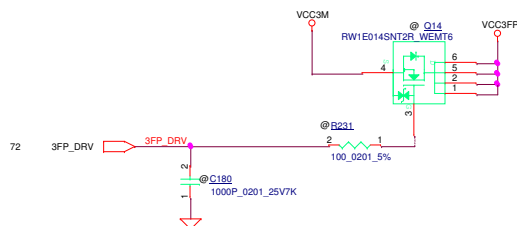
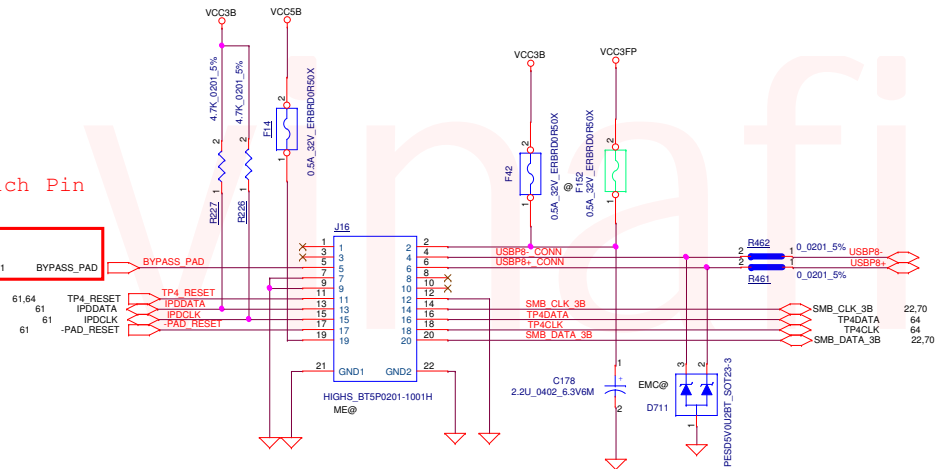


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				Date:	Tuesday, December 20, 2016 [Sheet 64 of 100]	






61 BYPASS\_PAD



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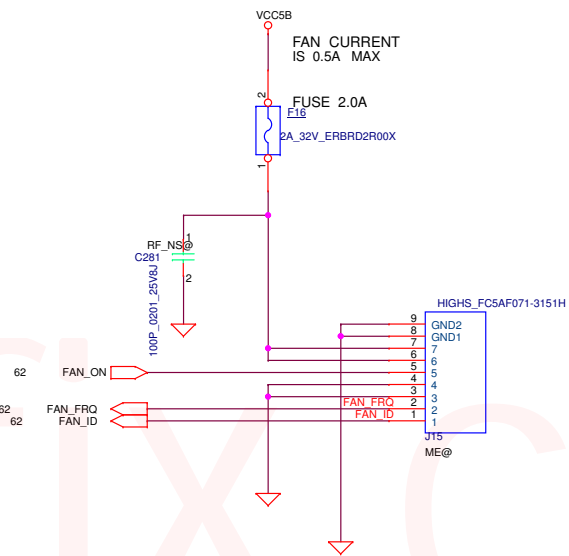
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			Date: Tuesday, December 20, 2016	
			Sheet	66 of 100



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**WOLVERINE4 UMA**

Rev 0.3

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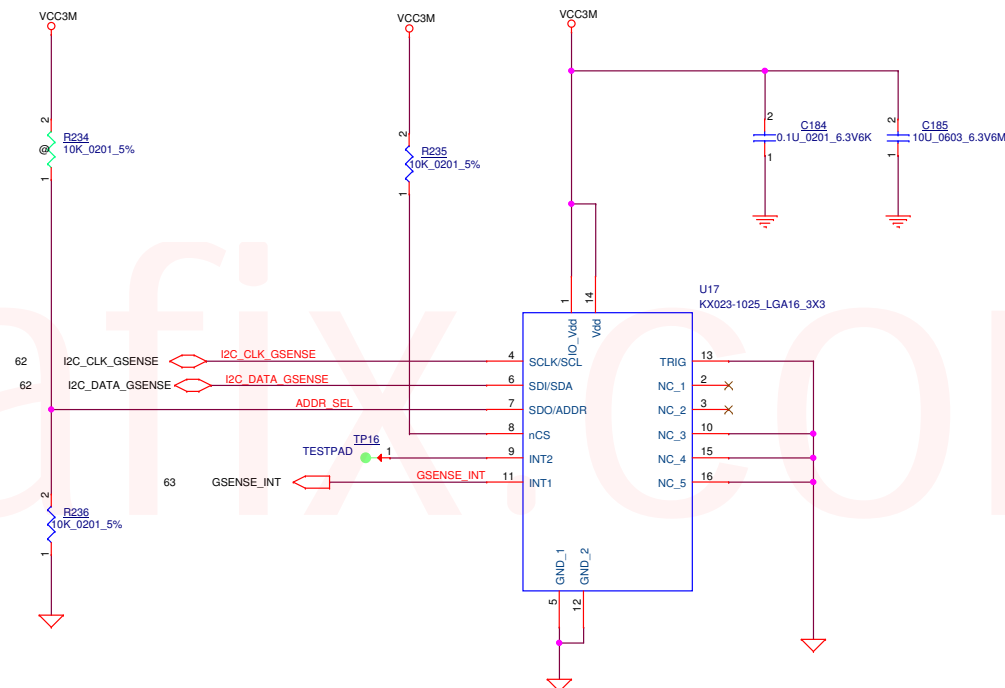


U17 PIN8 nCS SPI enable / I2C mode select TABLE

U17 PIN8 nCS	Mode Selection
H	I2C Mode
L	SPI Mode

G-SENSOR TABLE

LCFC P/N	ADDR_SEL	Address
LIS3DH SA00007Q700	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX023-1025 SA000073P00	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

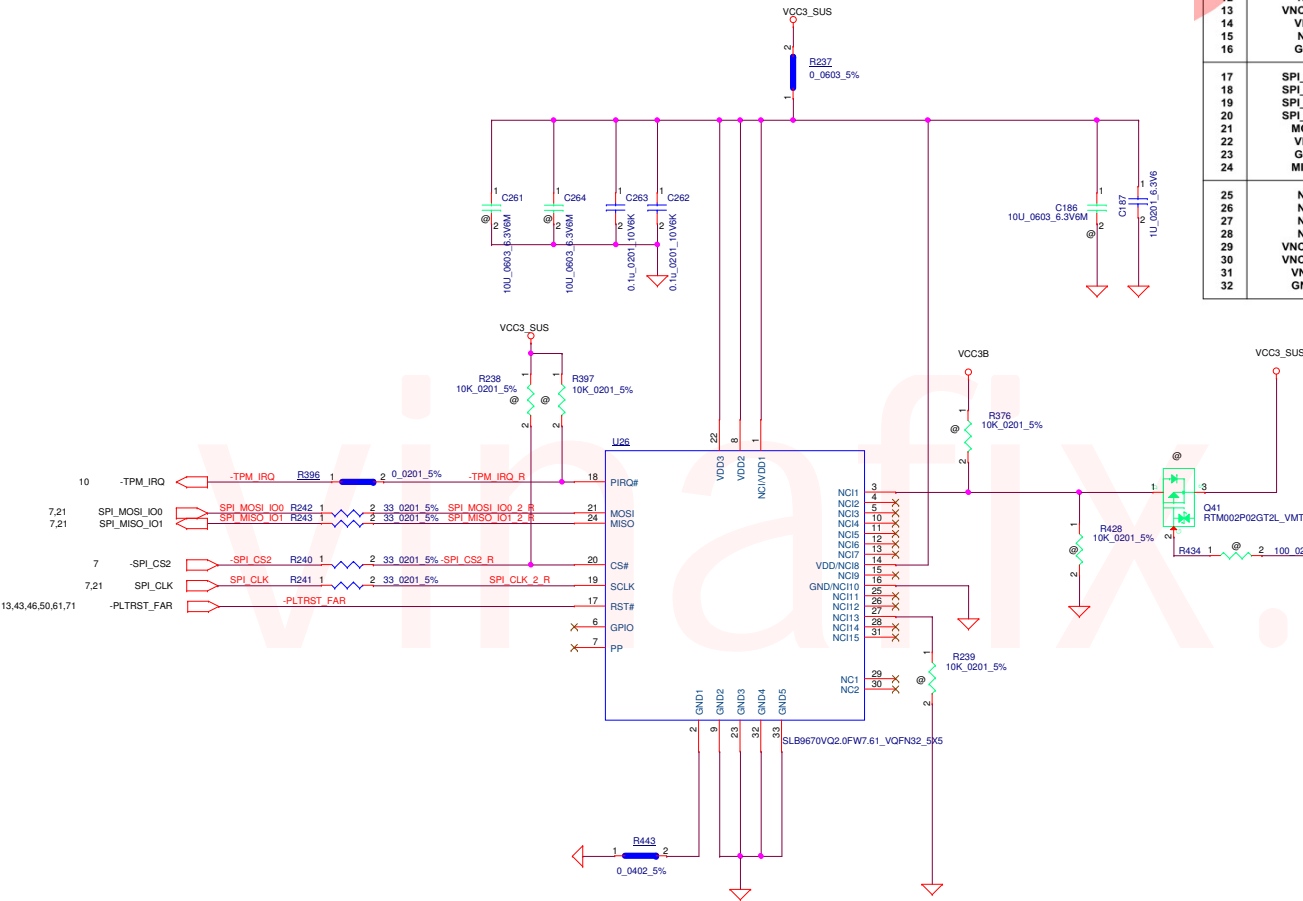


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Title		G-SENSOR	
Size	Document Number	VOLVERINE4 UMA	
Custom			
Date:	Tuesday, December 20, 2015	Sheet	68 of 100

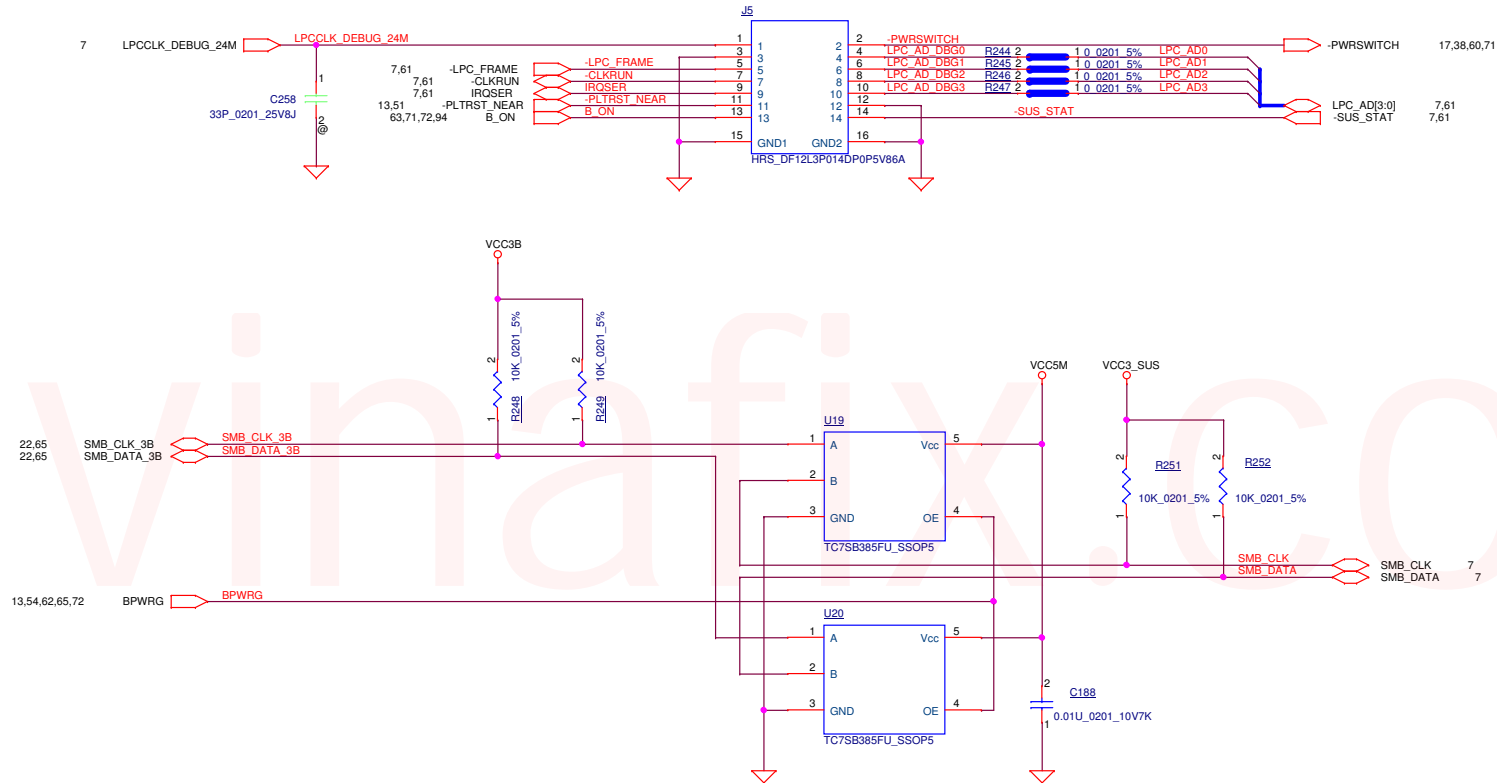
TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPC1650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	NC	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND




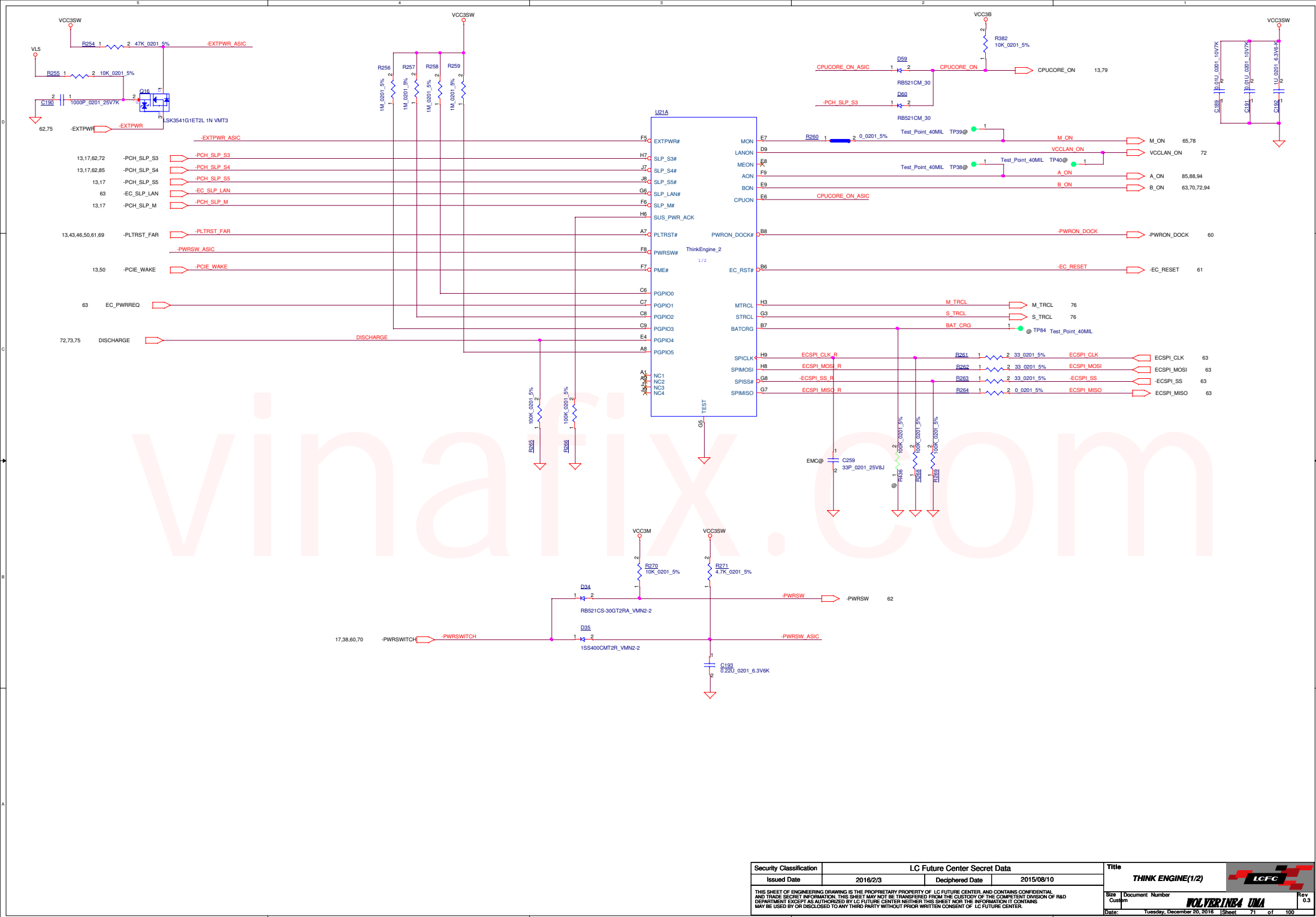
LPC Debug port

	Planner Only	BOX
J5	ASM	NO_ASM
RC29	ASM	ASM



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Title		
SMBUS SW/LPC DEBUG PORT		
Size	Document Number	Rev
Custom	<b>WOLVERINE4 UMA</b>	0.3
Date:	Tuesday, December 20, 2016	Sheet 70 of 100











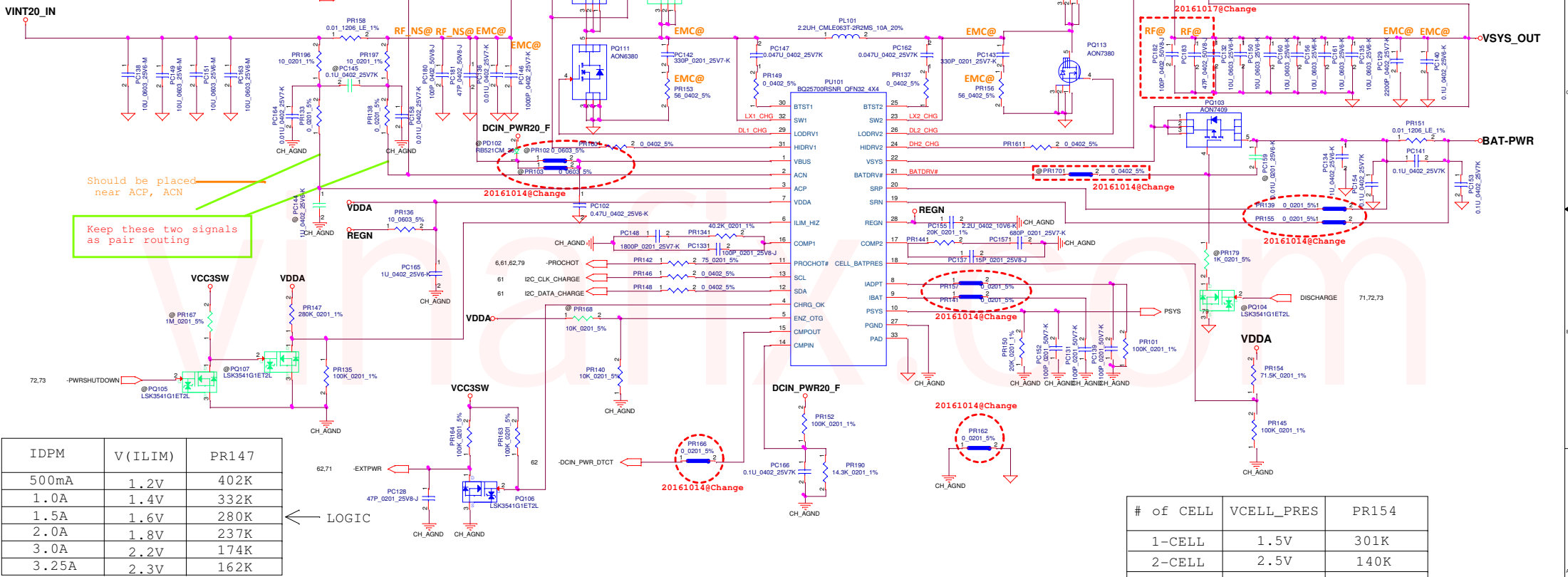
MLCCs must be placed symmetrically on Top and Bottom.

MLCCs must be placed symmetrically on Top and Bottom.

Table PL101  
 TOKIN : MPLCG0630L2R2  
 TDK : SPM6530T-2R2M  
 Cyntec : PCMB063T-2R2MS

Should be placed near ACP, ACN

Keep these two signals as pair routing

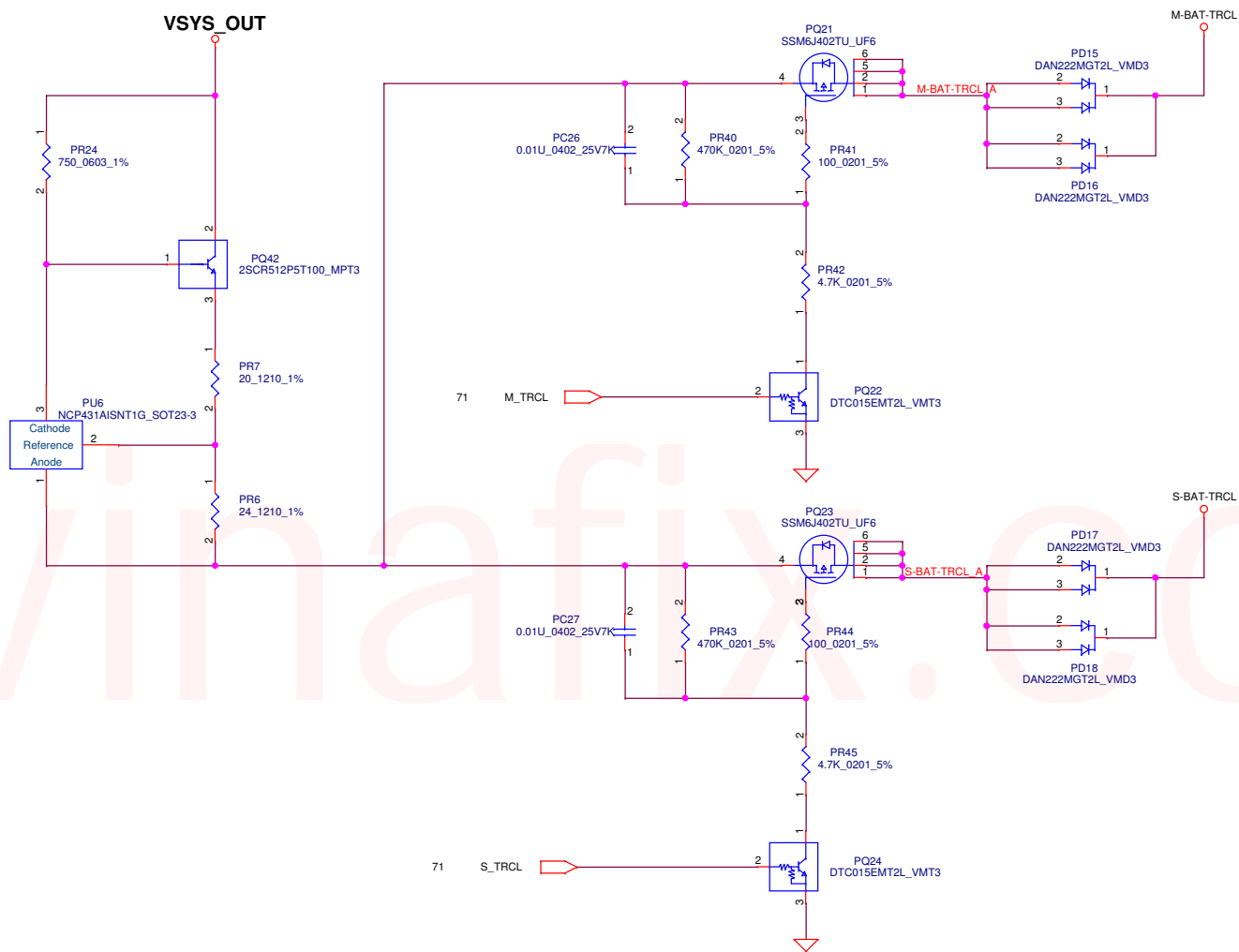



IDPM	V (ILIM)	PR147
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

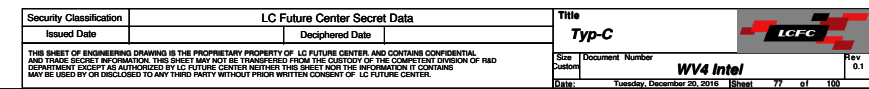
← LOGIC

# of CELL	VCELL_PRE	PR154
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

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				WV4 Intel	
				Date:	Tuesday, December 20, 2016
				Sheet	76 of 100
				Rev	0.24

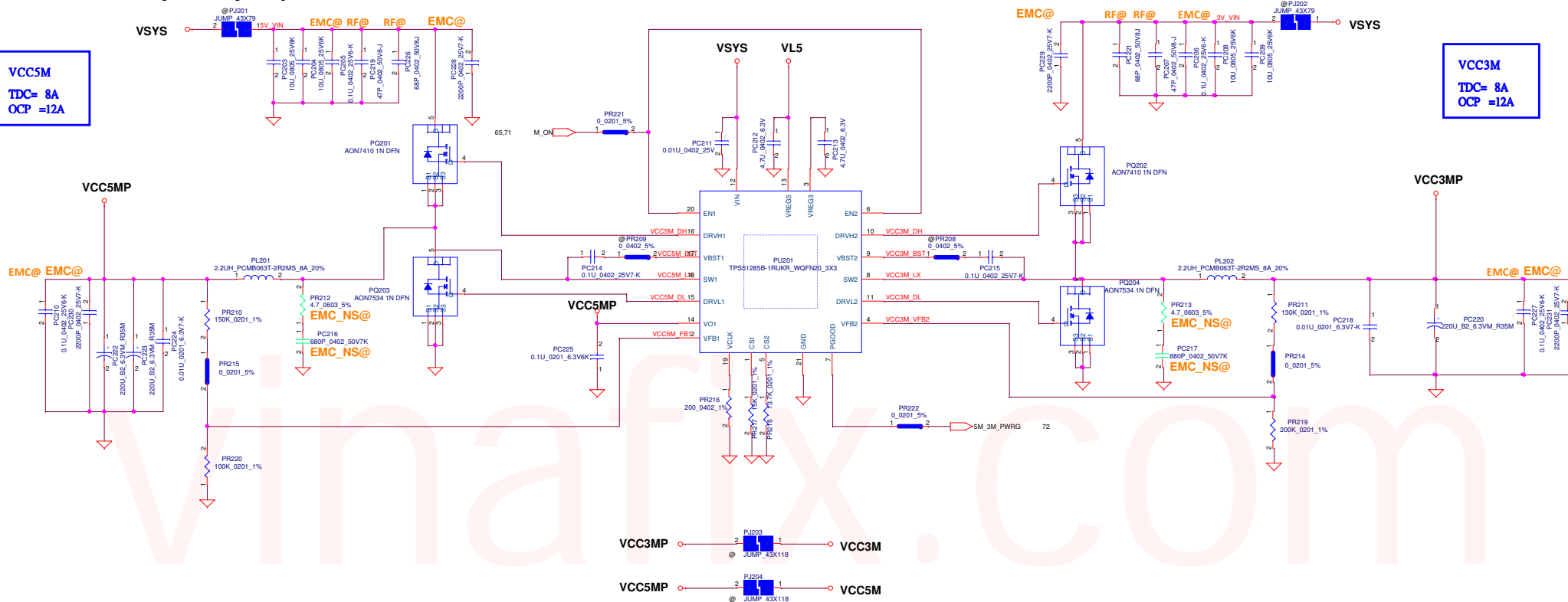


All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

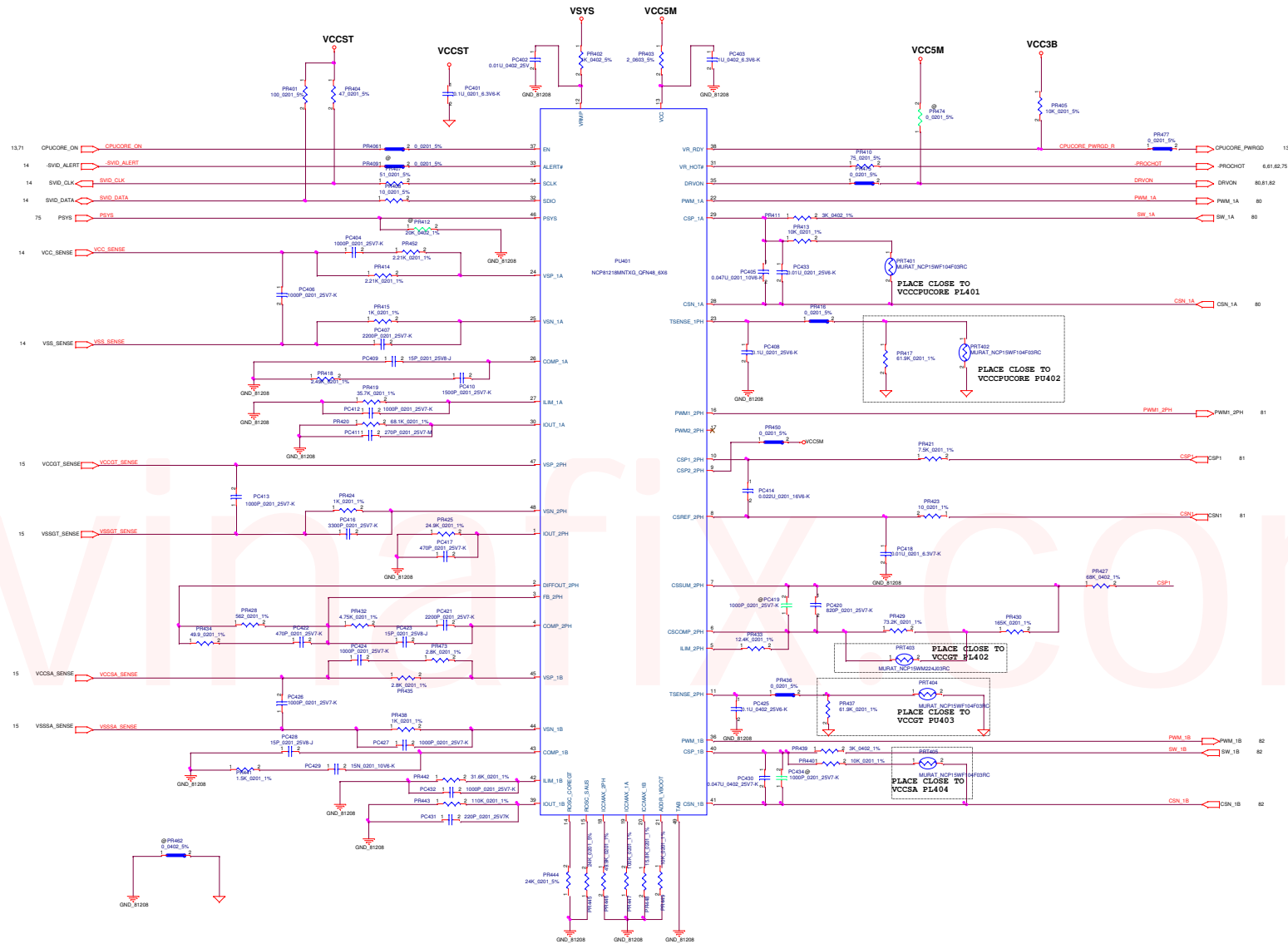
VCC5M  
TDC= 8A  
OCP =12A

VCC3M  
TDC= 8A  
OCP =12A



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Sheet	WV4 Intel	0.1	
Date	Tuesday, December 28, 2016	Sheet	78 of 100









6pcs 22uF for VCCSA

VCCSA

PC580 22U\_0603 6.3V6M

PC582 22U\_0603 6.3V6M

PC582 22U\_0603 6.3V6M

PC583 22U\_0603 6.3V6M

PC584 22U\_0603 6.3V6M

PC589 22U\_0603 6.3V6M


VCCSA

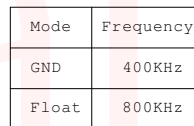
PC537 22U\_0603 6.3V6M


PC538 22U\_0603 6.3V6M

PC539 22U\_0603 6.3V6M

VCCSA



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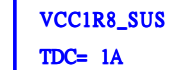
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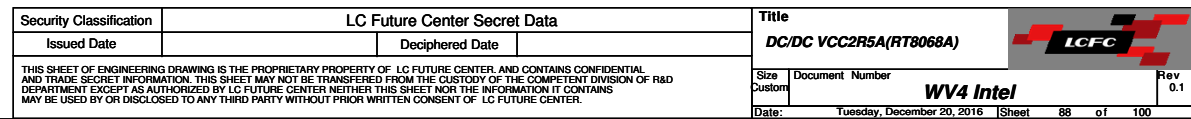


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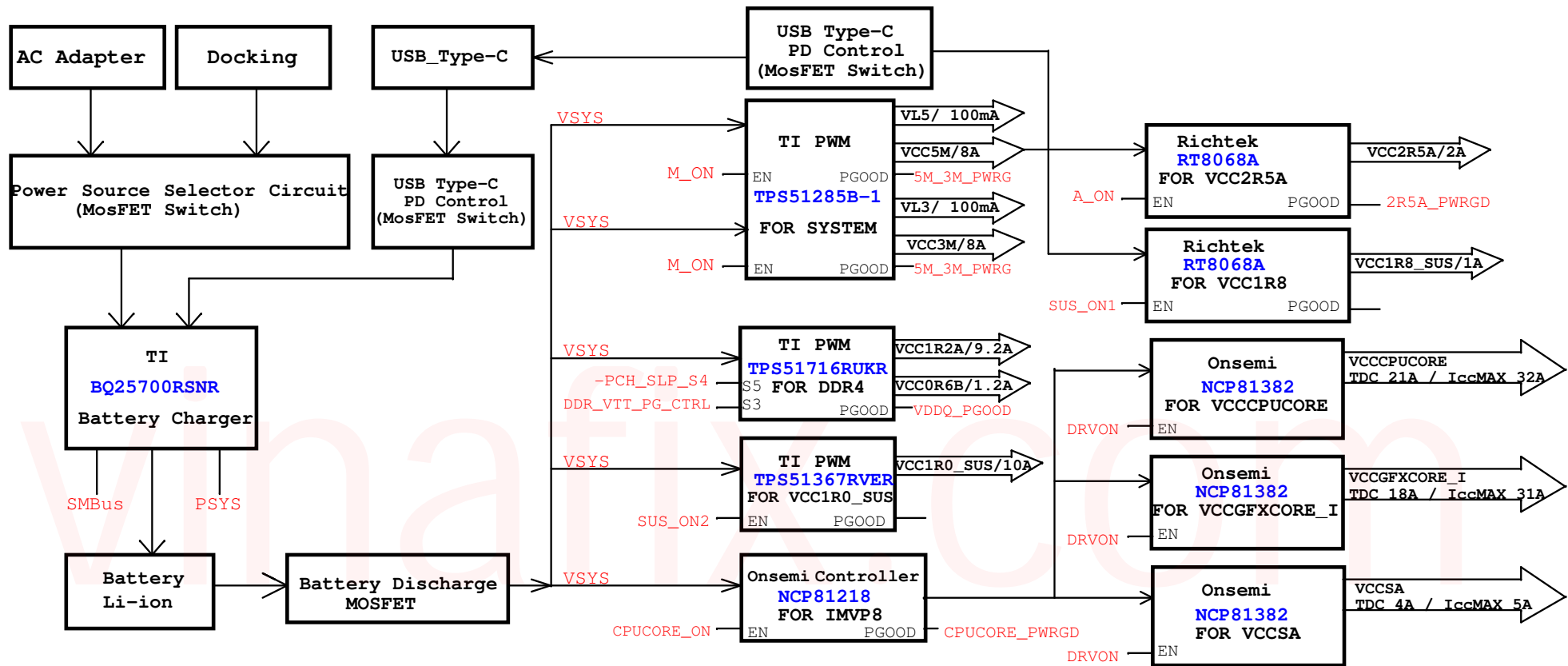
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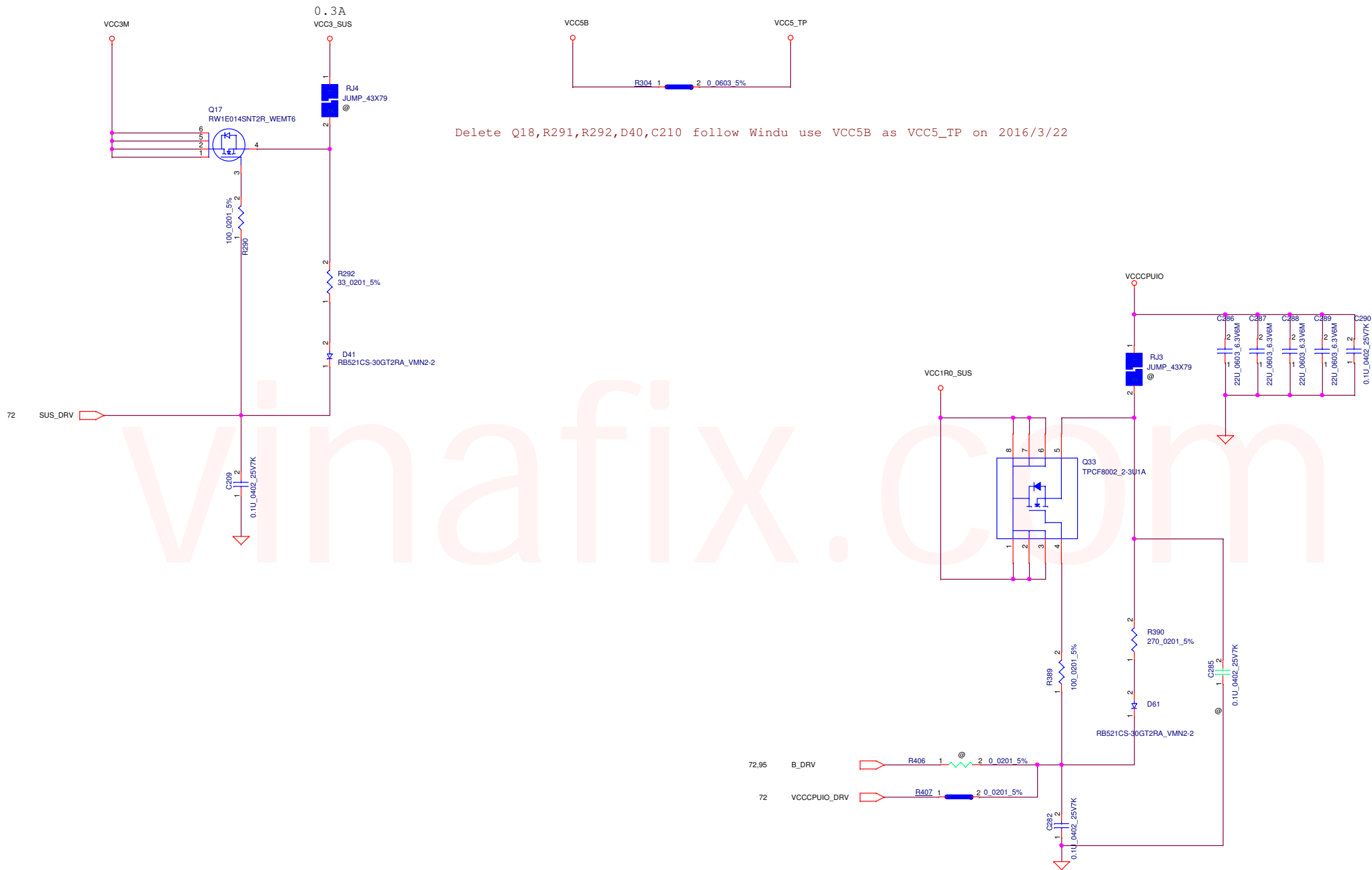
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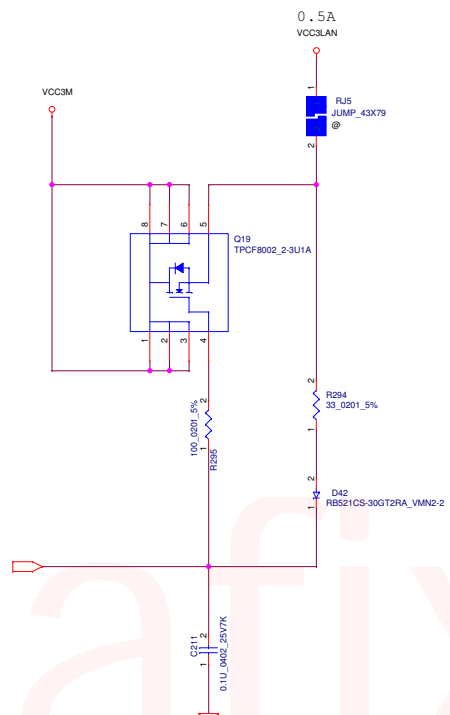
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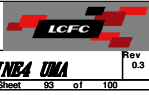


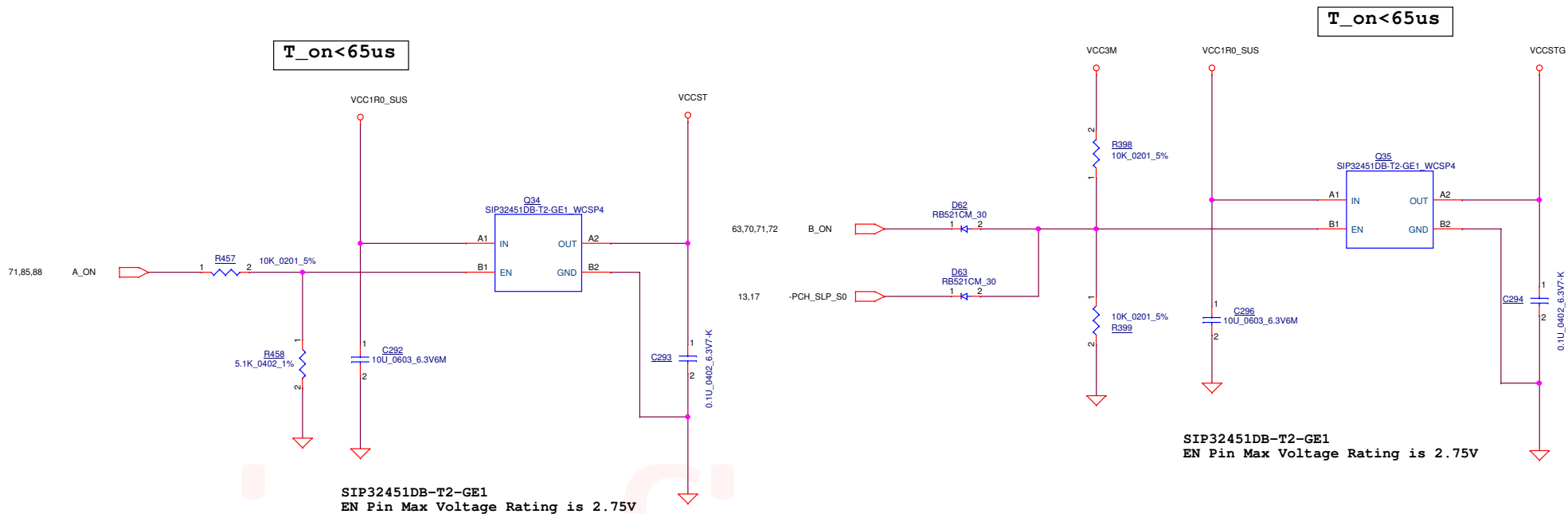
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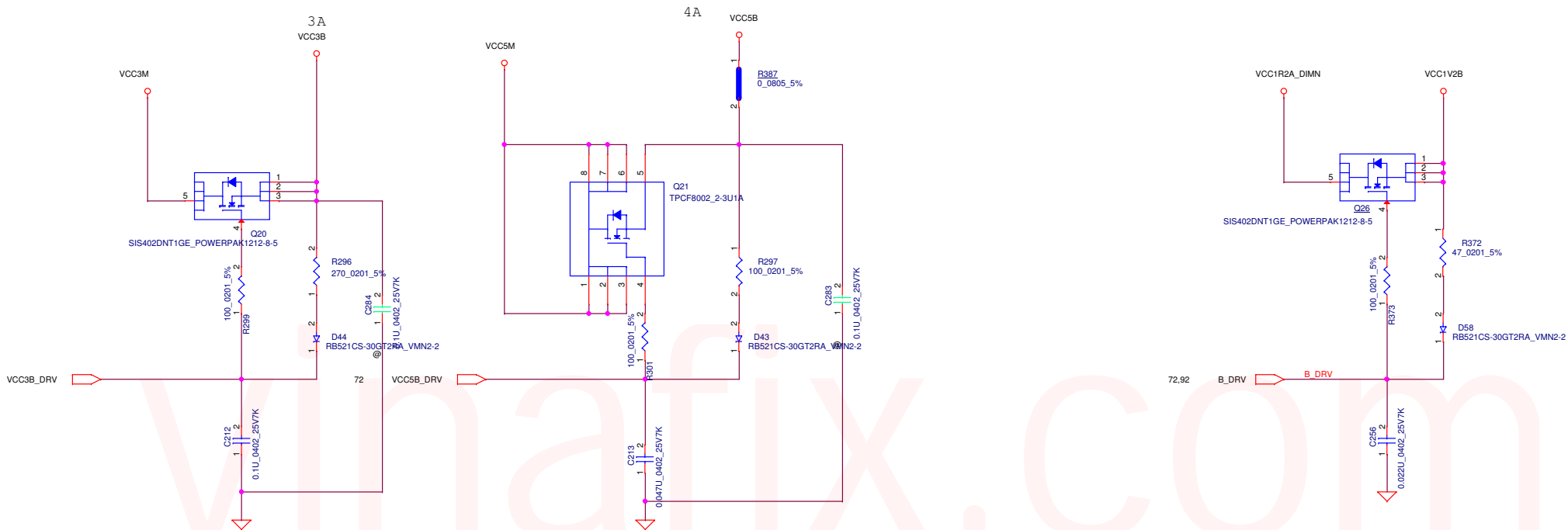
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Date:	Tuesday, December 20, 2016	Sheet	92 of 100




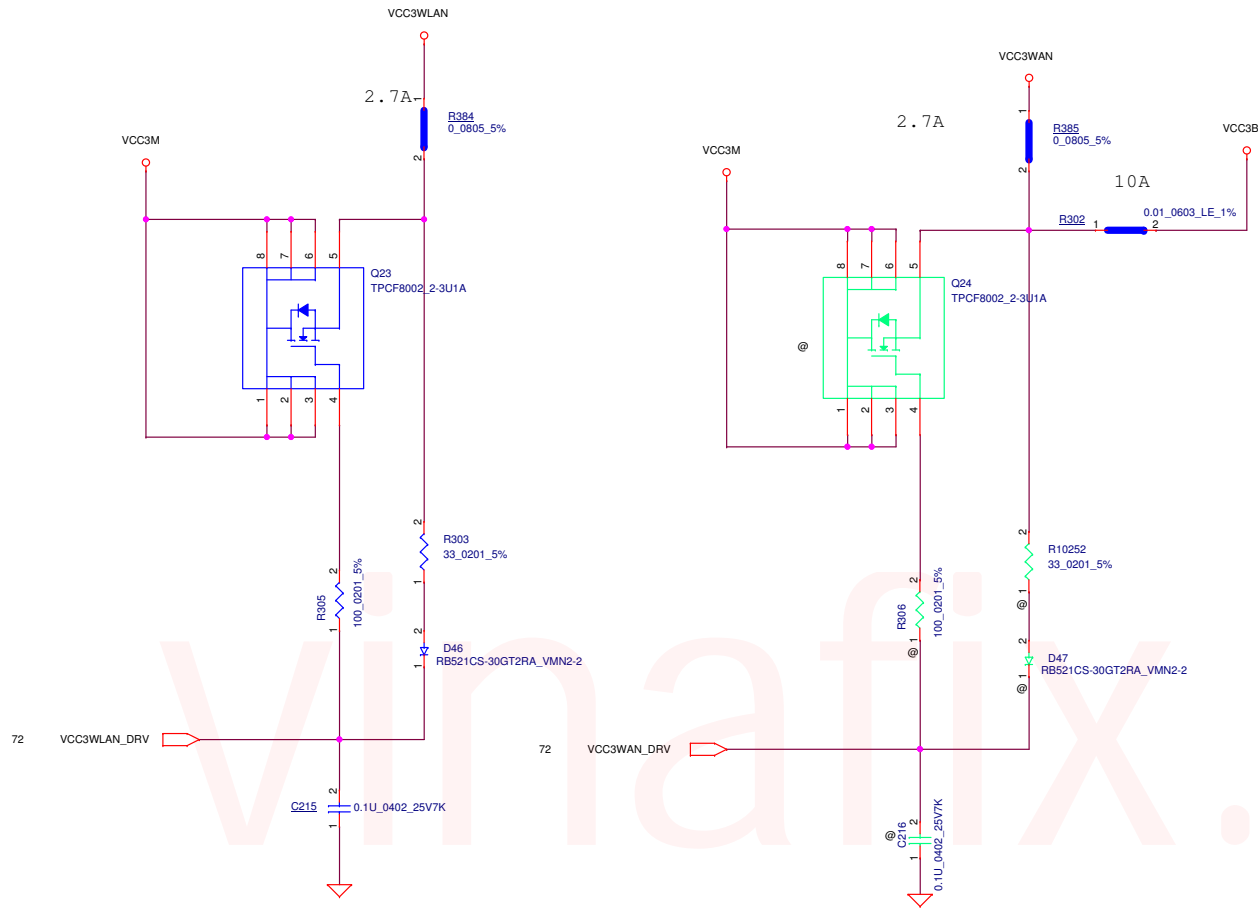
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						Date:	Tuesday, December 20, 2016	Sheet 95 of 100



TABLE

AOAC	YES	NO
R1055	NO-ASM	ASM
Q94	ASM	NO-ASM
R8924	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM



↑  
LOGIC

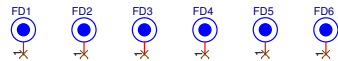
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			Date	Tuesday, December 20, 2018 15:00	100 of 100